



- Tentative Specification
- **Preliminary Specification**
- Specification Approval

Specification For SID 7.50” BWR EPD

Model Name: SE0750MNW11-TNG-A0

Version:V0.1

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Notes:		

Notes :

- 1、 Please contact SID before assigning your product based on this module specification.
- 2、 To improve the quality of product, and this product specification is subject to change without any notice.

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1. Over View

SE0750MNW11-A0 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 7.5" active area contains 800×480 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 800×480 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in flash memory
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C Signal Master Interface to read external temperature sensor/ built-in temperature sensor
- Available in COG package IC thickness 280um

3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	800 (H)×480(V)	Pixel	Dpi:124
Active Area	163.20(H)×97.92(V)	mm	
Pixel Pitch	0.204×0.204	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.20(H)×111.20 (V) ×1.12 (D)	mm	
Weight	42	g	

6. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSHR	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	Keep Open
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	Keep Open
8	BS1	I	Bus Interface selection pin	Note 6-5
9	BUSY	O	Busy state output pin	Note 6-4
10	RES	I	Reset signal input. Active Low.	Note 6-3
11	D/C	I	Data /Command control pin	Note 6-2
12	CS	I	Chip select input pin	Note 6-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C =Capacitor Pin

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 6-3: This pin (RST) is reset signal input. The Reset is active Low

Note 6-4: This pin (BUSY) is BUSY state output pin. When BUSY is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put BUSY pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 6-5: Table: Bus interface selection

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

7. MCU Interface

7.1 MCU interface selection

It can support 3-wire/4-wire serial peripheral interface. In the Module, The MCU interface is pin select-able by BS1 pins shown in.

Table 7-1: MCU interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wireSPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Figure 7-2.

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

- (1)L is connected to VSS and H is connected to VDDIO
- (2)↑ stands for rising edge of signal

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

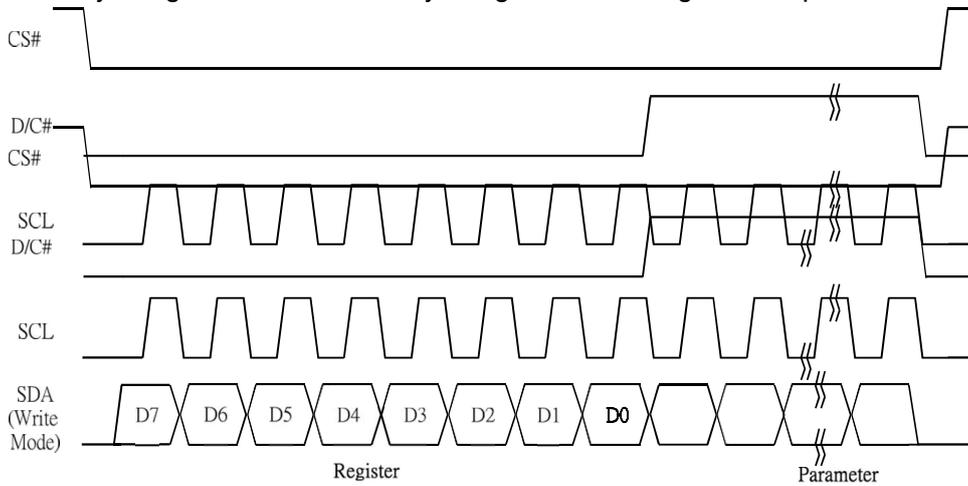


Figure 7-1: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

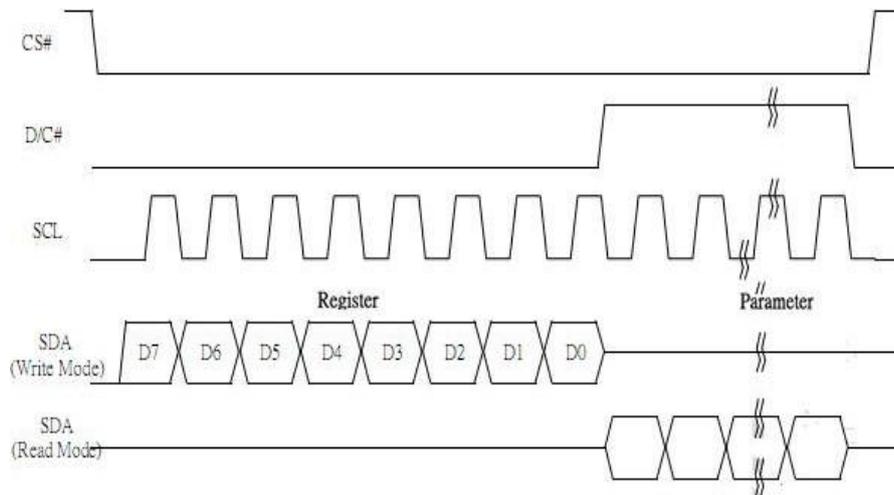


Figure 7-2: Read procedure in 4-wire SPI mode

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ...D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(2)L is connected to V_{SS} and H is connected to V_{DDIO}

(3)↑ stands for rising edge of signal

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. shows the write procedure in 3-wire SPI

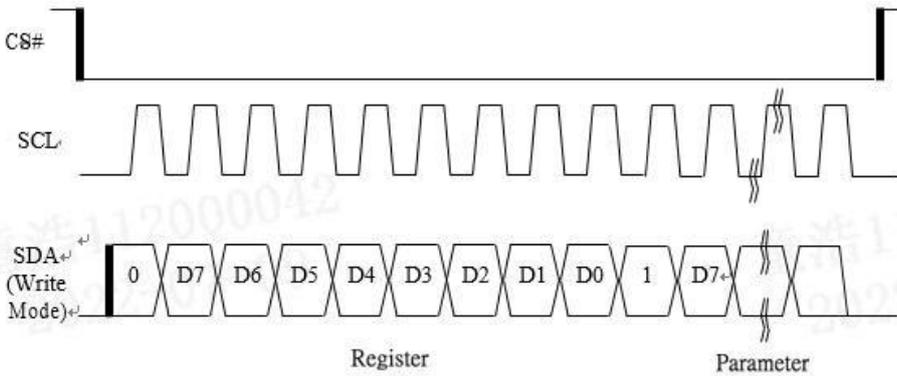


Figure 7-3: Write procedure in 3-wire SPI mode

In the Read mode:

- 1.After driving CS# to low, MCU need to define the register to be read.
- 2.D/C#=0 is shifted thru SDA with one rising edge of SCL
- 3.SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7,D6, ...D0.
- 4.D/C#=1 is shifted thru SDA with one rising edge of SCL
- 5.SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, ... D0.
- 6.Depend on register type, more than 1 byte can be read out. After all byte are read,CS# need to drive to high to stop the read operation.

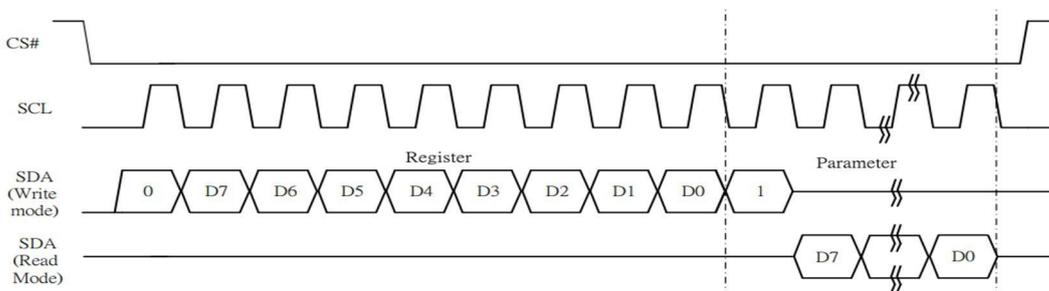
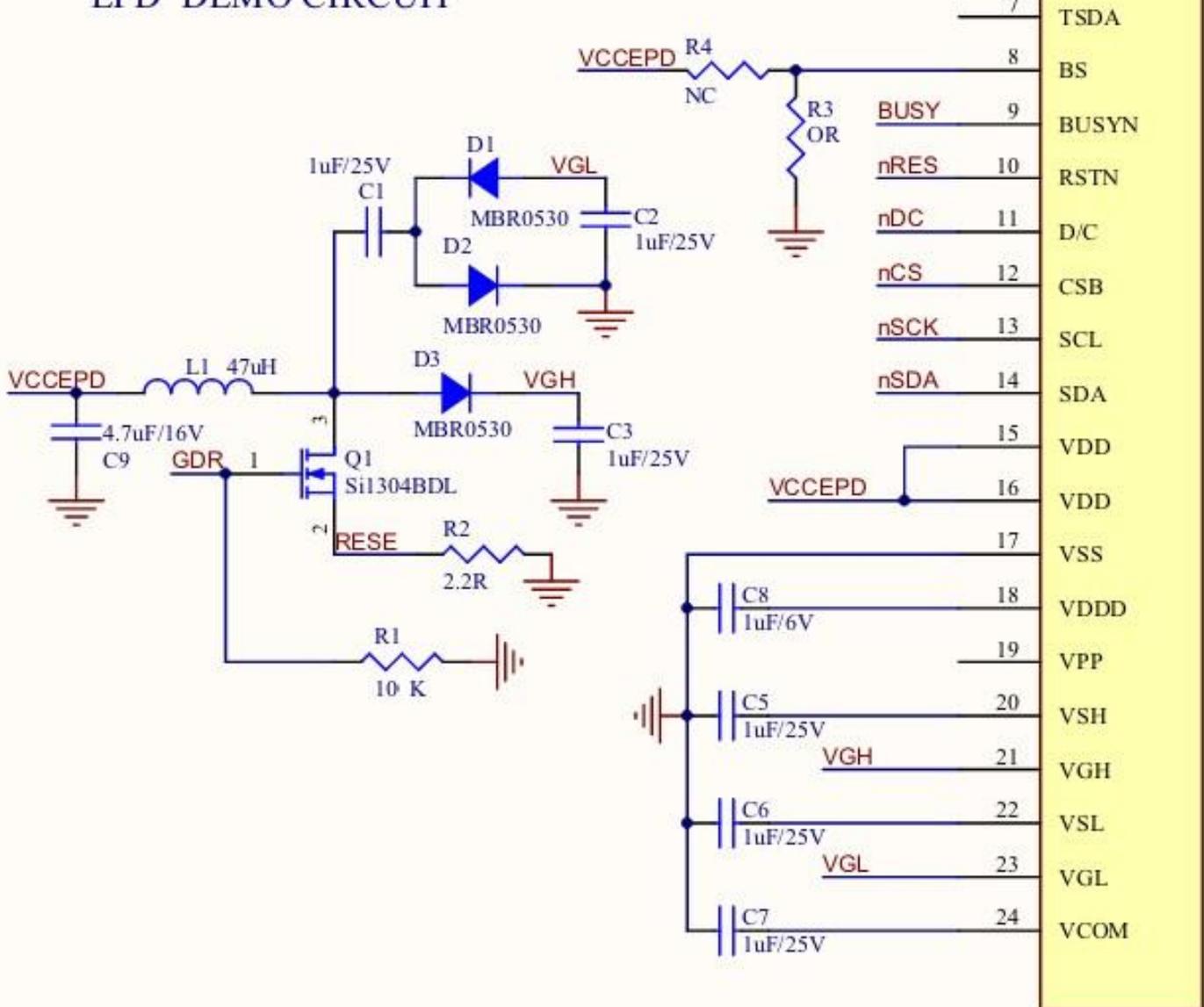


Figure 7-4: Read procedure in 3-wire SPI mode

8. Reference Circuit

EPD DEMO CIRCUIT



9. Absolute Maximum Rating

Table 9-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V _{CI}	Logic supply voltage	-0.3 to +6.0	V	-	-	
T _{OPR}	Operation temperature range	0 to 40	°C	45 to 70	%	Note 9-1
T _{ttg}	Transportation temperature range	-25 to 60	°C	45 to 70	%	Note 9-2
T _{stg}	Storage condition	0 to 40	°C	45 to 70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to 70	%	

Note 9-1: We guarantee the single pixel display quality for 0-35°C, but we only guarantee the bar code readable for 35-40°C. Normal use is recommended to refresh every 24 hours.

Note 9-2: T_{ttg} is the transportation condition, the transport time is within 10 days for -25°C~0°C or 40°C~60°C.

Note 9-3: When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months.

10. DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.3V, T_{OPR}=25°C.

Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V _{CI}	V _{CI} operation voltage	-	V _{CI}	2.3	3.3	3.6	V
V _{IH}	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.7V _{IO}		V _{IO}	V
V _{IL}	Low level input voltage	-		GND	-	0.3V _{DDIO}	V
V _{OH}	High level output voltage	I _{OH} = 400uA	BUSY	V _{IO} -0.4	-	-	V
V _{OL}	Low level output voltage	I _{OL} = -400uA		GND	-	GND+0.4	V
I _{update}	Module operating current	-	-	-	TBD	-	mA
I _{sleep}	Deep sleep mode (POWER OFF MODE)	V _{CI} =3.3V	-	-	-	3	uA

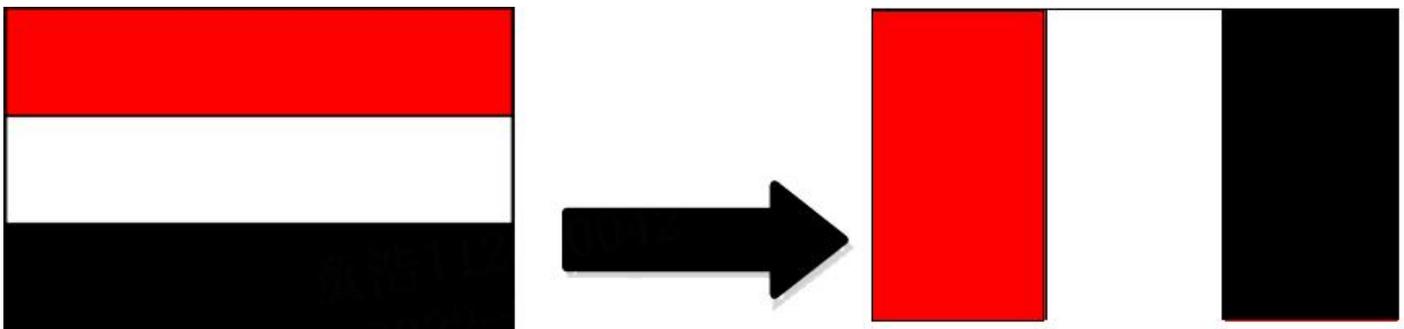
The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 10-1)

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

- V_{com} value will be OTP before in factory or present on the label sticker.

Note 10-1

The Typical power consumption



11. Serial Peripheral Interface Timing and Command Table

11.1 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.3V to 3.6V, T_{OPR}=25°C, CL=20pF

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

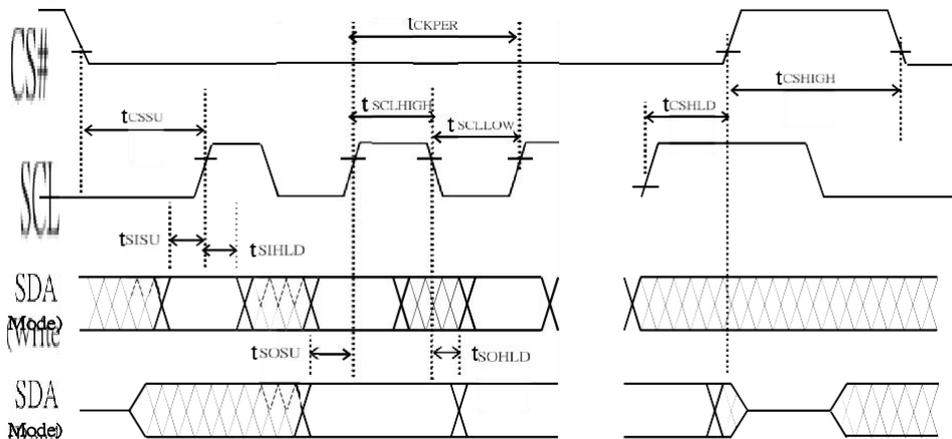


Figure 11-1: SPI timing diagram

11.2 Command Table

Please refer to IC Spec.

12. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	TBD	-	mAs	-
Deep sleep mode	-	25°C	-	3	uA	POWER OFF MODE

mAs=update average current × update time (Please refer to the actual test results)

13. Power ON/OFF Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power ON Sequence

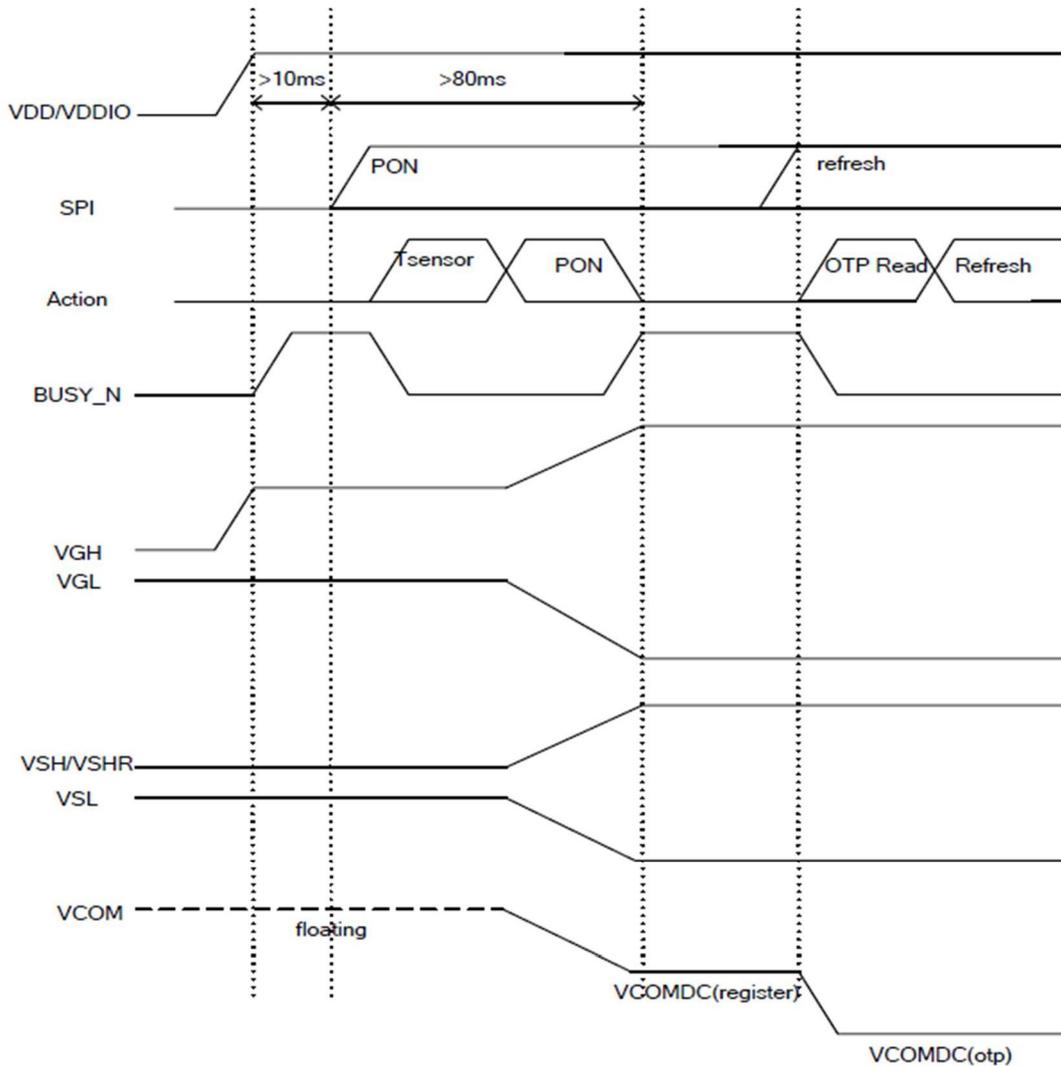


Figure 1: Power on sequence

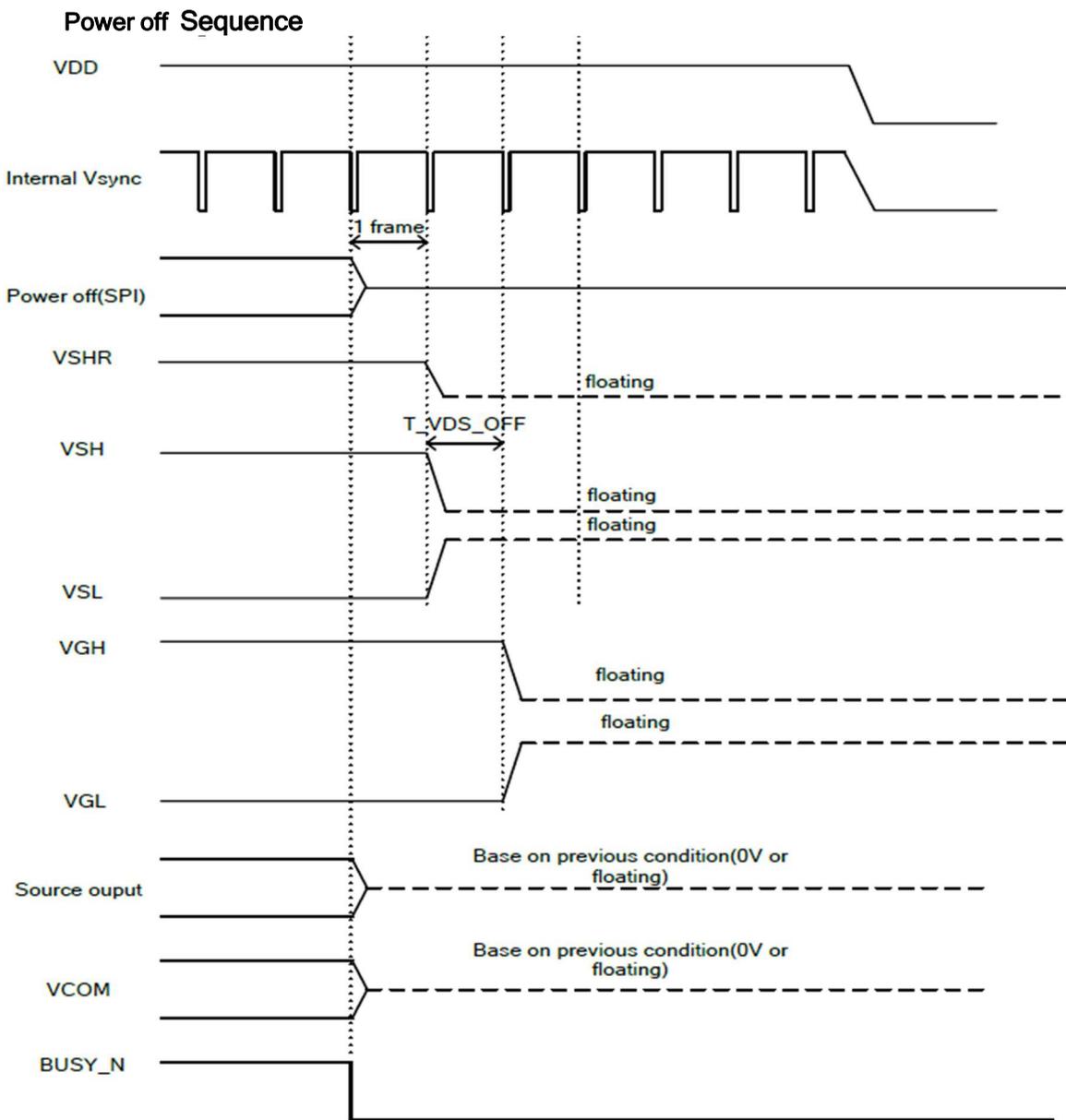


Figure 2: Power off sequence

14. Optical characteristics

14.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
KS	Black State L* value		-	-	14		Note 14-1
	Black State a* value		-	-	5		Note 14-1
WS	White State L* value		62	65	-		Note 14-1
RS	Red State L* value	Red	25	28	-		Note 14-1
	Red State a* value	Red	36	40	-		Note 14-1
Panel' s life	-	0°C~40°C		5years	-	-	Note 14-2
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state, RS: Red state

Note 14-1 : Luminance meter : i - One Pro Spectrophotometer

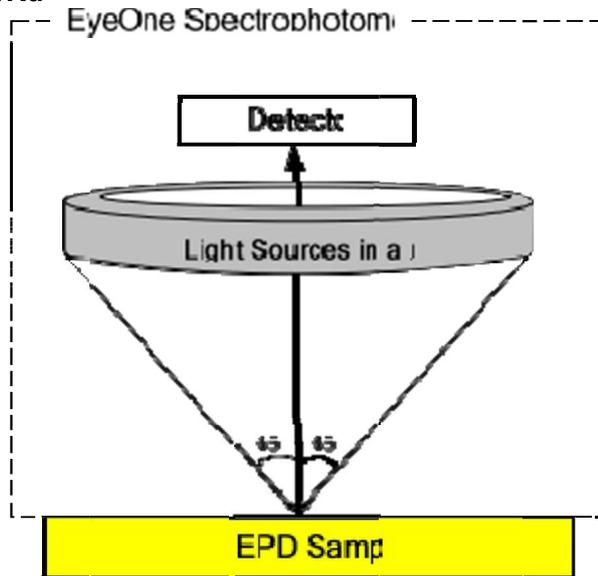
Note 14-2: We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH; Suggest Updated once a day;

Note 14-3: To increases the black and white screen clear screen when red has refreshed for a long time , the effect is better.

14.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd):

R1: white reflectance Rd: dark reflectance
 $CR = R1/Rd$

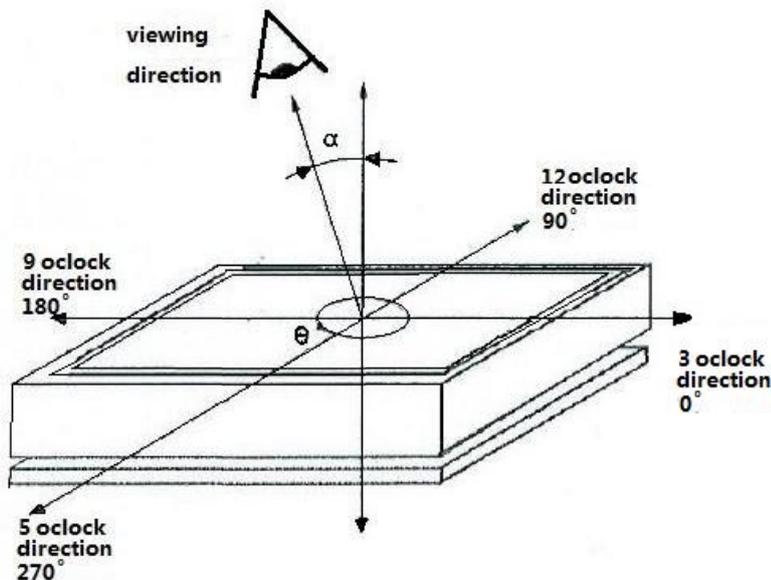


14.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard whiteboard. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



15. Handling, Safety and Environmental Requirements

WARNING

The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status

Product specification

The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
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Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification
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ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

16. Reliability test

	TEST	CONDITION	REMARK	
1	High-Temperature Operation	T=50°C, RH=30%RH, For 240Hr		
2	Low-Temperature Operation	T = 0°C for 240 Hr		
3	High-Temperature Storage	T=60°C RH=35%RH For 240Hr	Test in white pattern	
4	Low-Temperature Storage	T = -25°C for 240 Hr	Test in white pattern	
5	High Temperature, High-Humidity Operation	T=40°C, RH=90%RH, For 168Hr		
6	High Temperature, High-Humidity Storage	T=60°C, RH=80%RH, For 240Hr	Test in white pattern	
7	Temperature Cycle	-25°C (30min)~60°C (30min), 50 Cycle	Test in white pattern	
8	Package Vibration	1.04G, Frequency : 20~200Hz Direction : X, Y, Z Duration: 30 minutes in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence: 1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment	
10	Electrostatic discharge	HBM: 330 Ω, 150pF	Air +/-4KV; Contact +/-2KV	

Actual EMC level to be measured on customer application.

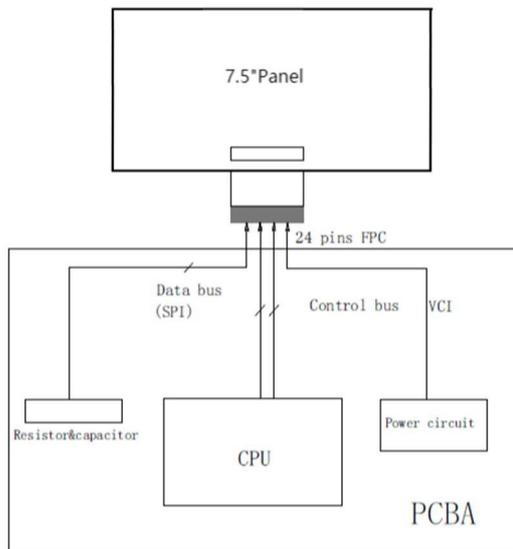
Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white/red pattern, hold time is 150S.

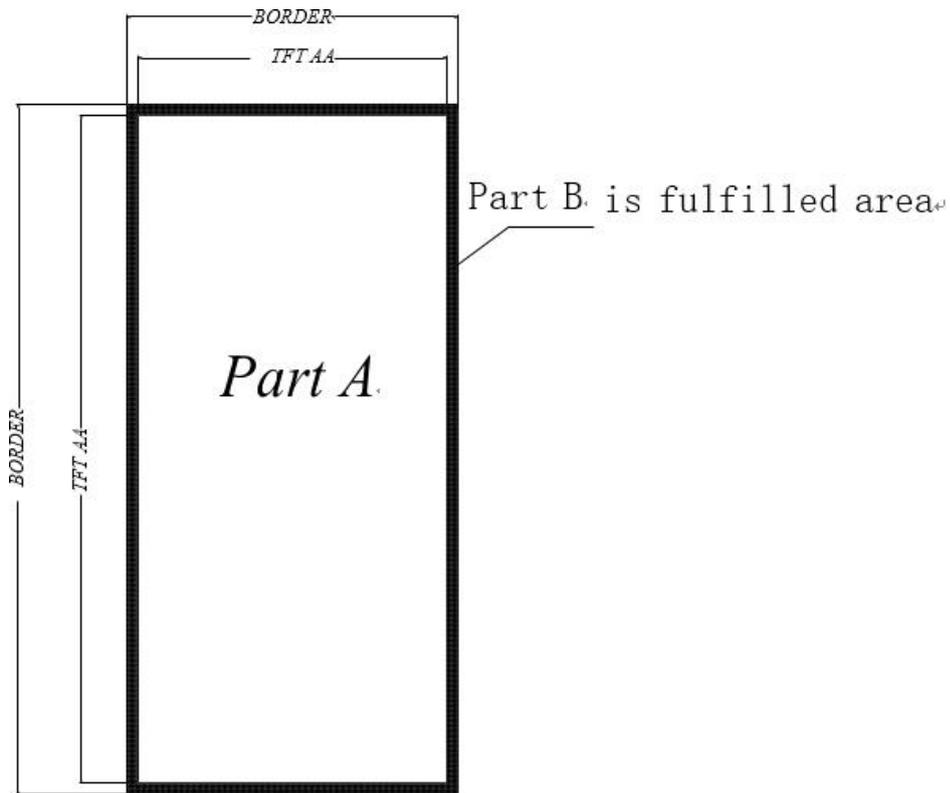
Note3: The function, appearance, opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C

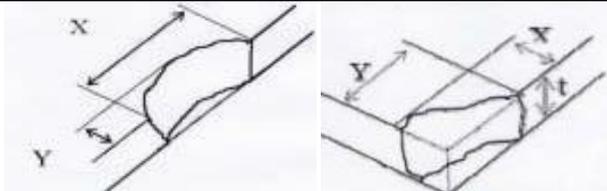
17. Block Diagram



18. PartA/PartB Specification



19. Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	170.20(H)×111.20 (V) ×1.12(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19°C ~25°C	55%±5 %RH	600~1200Lux	300 mm	35Sec	
Defect type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.2 mm		Ignore	Ignore	
		0.2mm < D ≤ 0.4 mm		N≤4	Ignore	
		0.4mm < D ≤ 0.6 mm		N≤1	Ignore	
		D>0.6mm		Not Allow		
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.1 mm		Ignore	Ignore	
		1.0mm < L ≤ 9.0mm, 0.1 < W ≤ 0.2mm,		N≤2	Ignore	
		L > 9 mm, W > 0.2mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.4mm		Ignore	Ignore	
		0.4mm ≤ D ≤ 0.6mm		N≤4	Ignore	
		D > 0.6 mm		Not Allow	Ignore	
Side Fragment	Visual/Film card	Do not affect the electrode circuit (Edge chipping) X≤8mm, Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
						
Remark	1. Cannot be defect & failure cause by appearance defect;					
	2. Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					

Note1 : OQC inspection: One-time sampling plan for GB/T 2828.1-2012 , Inspection Level II, CR: AC/Re=0/1, MA=0.4,MI=0.65.

Note2: Spot define: That only can be seen under White State or Dark State defects

Note3: Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Note4:Any defect must be judged by Optical Microscope.

Note5:Here is definition of the “Spot” and “Scratch or line defect”

Spot: $W > 1/4L$

Scratch or line defect : $W \leq 1/4L$ Note6:Definition for L/W and D (major axis)

Note7: FPC bonding area pad doesn't allowed visual inspection

Note8:

