⦿ Tentative Specification

✓ Preliminary Specification

⦿ Specification Approval

Specification For SID 10.20" BWR EPD

Model Name: JS1020HN01-TNG-A0

Version:V0.1

SID	PREPARED BY	CHECKED BY	APPROVED BY
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DATE	20220319	20220319	20220319

CUSTOMER APPROVAL	SIGNATURE	DATE
	Notes:	

Notes :

1、Please contact SID before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	20220319	First release	Preliminary

CONTENTS

1. General Description

SE1020HN01-A0 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 10.2" active area contains 960×640 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

2. Features

- 960×640 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	10.2	Inch	
Display Resolution	960(H)×640V)	Pixel	Dpi:113
Active Area	215.52(H)×143.68(V)	mm	
Pixel Pitch	0.2245×0.2245	mm	
Pixel Configuration	Rectangle		
Outline Dimension	224.00(H)×157.00 (V) ×0.9(D)	mm	**Without masking film**
Weight	TBD	g	

5. Mechanical Drawing of EPD module

FRONT VIEW

SIDE VIEW

BOTTOM VIEW

TFT OD 224.00±0.2 *
TFT AA 215.52 *
TFT OD 157.00±0.2 *
TFT AA 143.68 *
4.22
4.24
98.55 *
0.15±0.03 *
0.50±0.03 *
11.50±0.05 *
12.50±0.1 *
31.30±0.1 *
3.00±0.2 *

Total 0.90±0.1 *
Edge Sealing
Silicon-Glue
IC
FPC 0.10±0.03
FPC+PI stiffener
Total Thickness 0.30±0.03 *

print white
mark line
PI stiffener T=0.2
6.00
40.00 *

NOTES :
1.DISPALY MODE 10.2" ARREY FOR EPD;
2.DRIVE IC:SSD1677
3.RESOLUTION:960source X 640gate;
4.pixel pitch:0.2245*0.2245
5.dpi:113
6.Material conform to the ROHS standard
5.Unspecified Tolerance:±0.20;
7. * as the focus control size

REV.:	DESCRIPTION	DATE
A0	Previous A0	

Signature	A0 confirmed	Date

ALL UNITS: mm
DWN:　DATE
CHK:　CUSTOMER NO.
APP:　P/N
SHEET:
DATE:
PROJECTION

6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage,VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is

pulled HIGH,the data will be interpreted as data. When the pin is pulled LOW, the data will be

interpreted as command.

Note 6-3: This pin (RES#) is reset signal input.   The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be

interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High

when thedriver IC is working such as:

- Outputting display waveform; or

- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection.   When it is "Low", 4-line SPI is selected.When it is "High", 3-line SPI (9 bits SPI) is selected.

7. MCU Interface
7.1 MCU interface selection

E102A04 can support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin. The interface pin assignment for different MCU interfaces is shown in Table 7-1.

Note
(1) L is connected to VSS
(2) H is connected to VDDIO

Table 7-1: Interface pin assignment for different MCU interfaces

MCU Interface	Pin Name						
	BS1	RES#	CS#	D/C#	SCL	SDI	SDO
4-wire serial peripheral interface (SPI)	L	Required	Required	Required	SCL	SDI	SDO
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	Required	L	SCL	SDI	SDO

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in

4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure in 4-wire SPI is

shown inFigure 7-1..

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDIpin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Figure 7-1: wire mode

In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled
low. Aftercommand byte sent, the following byte(s) read are data byte(s), so D/C# bit is then
pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output
SDO bit shifting sequence is D7,D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.
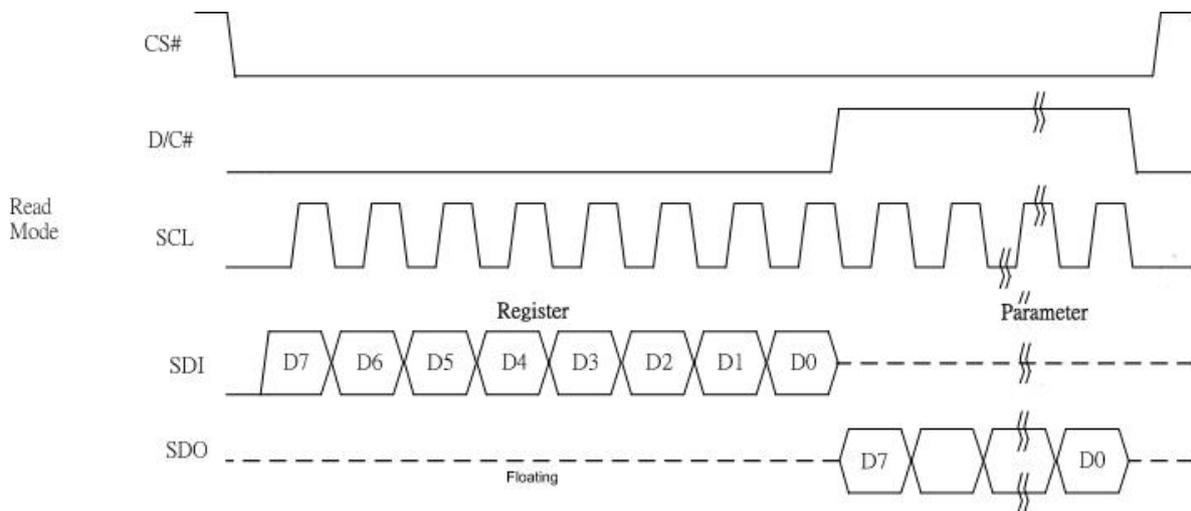
Figure 7-2: Read procedure in 4-wire SPI mode

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1,the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ stands for rising edge of signal
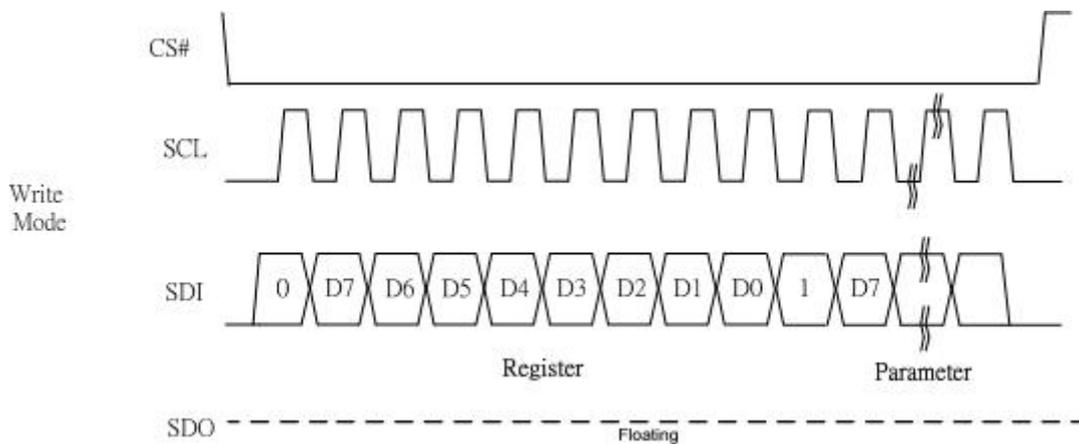
Figure 7-3: Write procedure in 3-wire SPI mode

In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0
bit. Figure 7-4 shows the read procedure in 3-wire SPI.
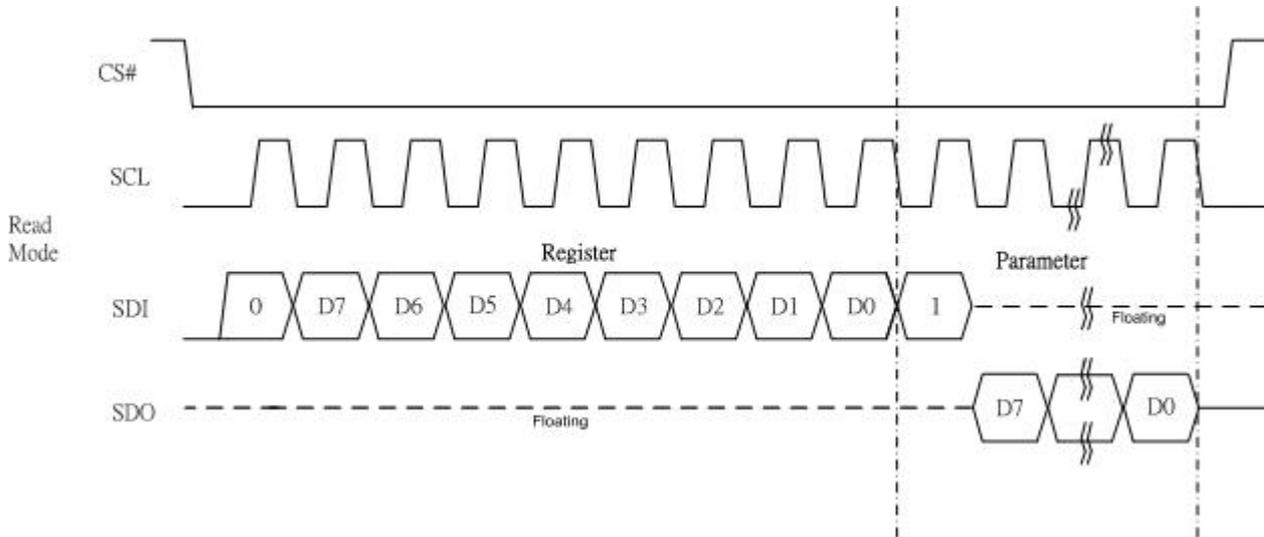
Figure 7-4: Read procedure in 3-wire SPI mode

8. COMMAND TABLE

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
						Command Table						
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[9:0]= 2A7h [POR], 680 MUX MUX Gate lines setting as (A[9:0] + 1).
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		B[2:0] = 000 [POR]. Gate scanning sequence and direction
0	1		0		0	0	0	B2	B1	B0		B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…679 (left and right gate interlaced) SM=1, G0, G2, G4 …G678, G1, G3, …G679 B[0]: TB TB = 0 [POR], scan from G0 to G679 TB = 1, scan from G679 to G0.
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 12V to 20V

A[4:0]	VGH	A[4:0]	VGH
00h	20	10h	16.5
07h	12	11h	17
08h	12.5	12h	17.5
09h	13	13h	18
0Ah	13.5	14h	18.5
0Bh	14	15h	19
0Ch	14.5	16h	19.5
0Dh	15	17h	20
0Eh	15.5	Other	NA
0Fh	16		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage
0	1		A7	A6	A5	A4	A3	A2	A1	A2		A[7:0] = 41h [POR], VSH1 at 15V
0	1		B7	B6	B5	B4	B3	B2	B1	B0		B[7:0] = A8h [POR], VSH2 at 5V.C[7:0] = 32h [POR], VSL at -15V
0	1		C7	C6	C5	C4	C3	C2	C1	C0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 17V8.8V

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

C[7] = 0,
VSL setting from -9V to -

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

Remark:
VSH1> VSH2

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gatedriver. The valid range is from 0 to 679.A[9:0] = 000h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		

When TB=0:
SCN [9:0] = A[9:0]
When TB=1:
SCN [9:0] = 679 - A[9:0]

											Command Table	
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control:
0	0		0	0	0	0	0	A2	A1	A0		After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 – Y decrement, X decrement, 01 – Y decrement, X increment, 10 – Y increment, X decrement, 11 – Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A2	A1	A0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detectionA[6:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high duringdetection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect
0	1		0	0	0	0	0	A2	A1	A0		The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCIdetection starts. BUSY pad will output high duringdetection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	0	18	0	0	0	1	1	0	0	0	Temperature SensorControl	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	1A	0	0	0	0	0	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register.A[11:0] = 7FFh[POR]
0	1		A11	A10	A9	A8	A7	A6	A5	A4		
0	1		A3	A2	A1	A0	0	0	0	0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A11	A10	A9	A8	A7	A6	A5	A4		
1	1		A3	A2	A1	A0	0	0	0	0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
							Command Table					
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR],A[7:6] A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option A[3:0] BW RAM option
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[3:0] BW RAM option

0000	Normal
0100	Bypass RAM content as 0
1000	Inverse RAM content

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

	Parameter (in Hex)
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	C7
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	CF
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1	90
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1	B0

												Description	Code
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 2	98
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2	B8
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	91
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	B1
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	99
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	B9
												Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	47
												Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	4F
												To Enable Clock Signal (CLKEN=1)	80
												To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)	C0
												Enable ANALOG Then DISPLAY with DISPLAY Mode 1	44
												Enable ANALOG Then DISPLAY with DISPLAY Mode 2	4C
												To DISPLAY with DISPLAY Mode 1	04
												To DISPLAY with DISPLAY Mode 2	0C
												To Disable ANALOG, then Disable Clock Signal (CLKEN=0, ANALOGEN=0)	03
												o Disable Clock Signal （CLKEN=0）	01

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		0	A6	0	0	A3	A2	A1	A0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

							Command Table					
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2B	0	0	1	0	1	0	1	1	Write Register forVCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytesD04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	58h	-2.2
0Ch	-0.3	5Ch	-2.3
10h	-0.4	60h	-2.4
14h	-0.5	64h	-2.5
18h	-0.6	68h	-2.6
1Ch	-0.7	6Ch	-2.7
20h	-0.8	70h	-2.8
24h	-0.9	74h	-2.9
28h	-1	78h	-3
2Ch	-1.1	7Ch	-3.1
30h	-1.2	80h	-3.2
34h	-1.3	84	-3.3
38h	-1.4	88	-3.4
3Ch	-1.5	8C	-3.5
40h	-1.6	90	-3.6
44h	-1.7	94	-3.7
48h	-1.8	98	-3.8
4Ch	-1.9	9C	-3.9
50h	-2	A0	-4
54h	-2.1		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2D	0	0	1	0	1	1	0	1	OTP Register ReadforDisplay Option	Read Register for Display Option:A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte G)[5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte H to Byte K)[4 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		

											Command Table	
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command for OTPcontent validation. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC readout Value
1	1		A15	A14	A13	A12	A11	A10	A9	A8		
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	36	0	0	1	1	0	1	1	0	Program OTPselection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1.Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register forDisplay Option	Write Register for Display Option B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode2 F[6]: PingPong for Display Mode 2F[7]: PingPong for Display Mode 11: Ping-Pong 0: Default G[7:0]~J[7:0] module ID /waveformversion. Remarks: A[7:0]~J[7:0] can be stored inOTP
0	1		0	0	0	0	0	0	0	0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	38	0	0	1	1	1	0	0	0	Write Register forUser ID	Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored inOTP
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		

								Command Table				
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A1	A0		
0	0	3A	0	0	1	1	1	0	1	0	Reserved	Reserved
0	0	3B	0	0	1	1	1	0	1	1	Reserved	Reserved
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option A [5:4] Fix Level Setting for VBD A [1:0] GS Transition setting for VBD
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[1:0]	VBD Transition
00[POR]	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0: Read RAM corresponding to 24h 1: Read RAM corresponding to 26h
0	1		0	0	0	0	0	0	0	A0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[9:0]: XSA[9:0], XStart, POR = 000h B[5:0]: XEA[9:0], XEnd, POR = 3BFh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		-	-	-	-	-	-	A9	A8		
0	1		0	0	B5	B4	B3	B2	B1	B0		
0	1		-	-	-	-	-	-	B9	B8		

												Command Table	
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	45	0	1	0	0	0	1	0	1	Set RAM Y-Address Start /End position	Specify the start/end positions of the window address in the Y direction by anaddress unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000hB[8:0]: YEA[8:0], YEnd, POR = 2A7h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		-	-	-	-	-	-	A9	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		-	-	-	-	-	-	B9	B8		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM For Regular Pattern	Auto Write RED RAM for Regular PatternA[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction accordingto Gate
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
												A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction accordingto Source
												BUSY pad will output high duringoperation.
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular PatternA[7:0] = 00h [POR] Auto Write B/W RAM for Regular PatternA[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
												A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction accordingto Source
												uring operation, BUSY pad will outputhigh.

Command Table													
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X addresscounter	Make initial settings for the RAM Xaddress in the address counter (AC)A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y addresscounter	Make initial settings for the RAM Yaddress in the address counter (AC)A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; itdoes not have any effect on the display module. However, it can be used to terminate Frame Memory Write or ReadCommands.

9. Reference Circuit

CON1
24Pin

Pin	Signal
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH
21	VGH
22	VSL
23	VGL
24	VCOM
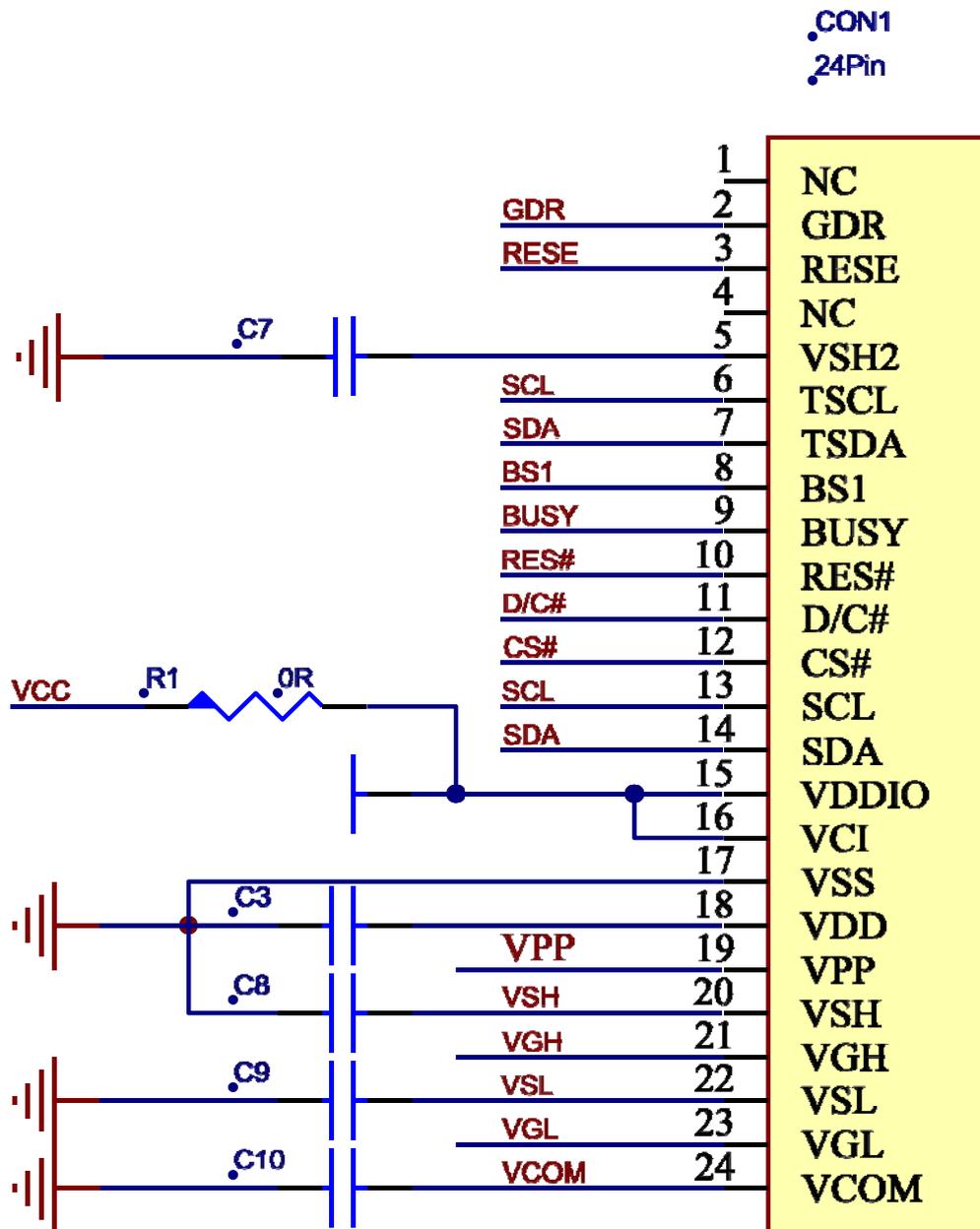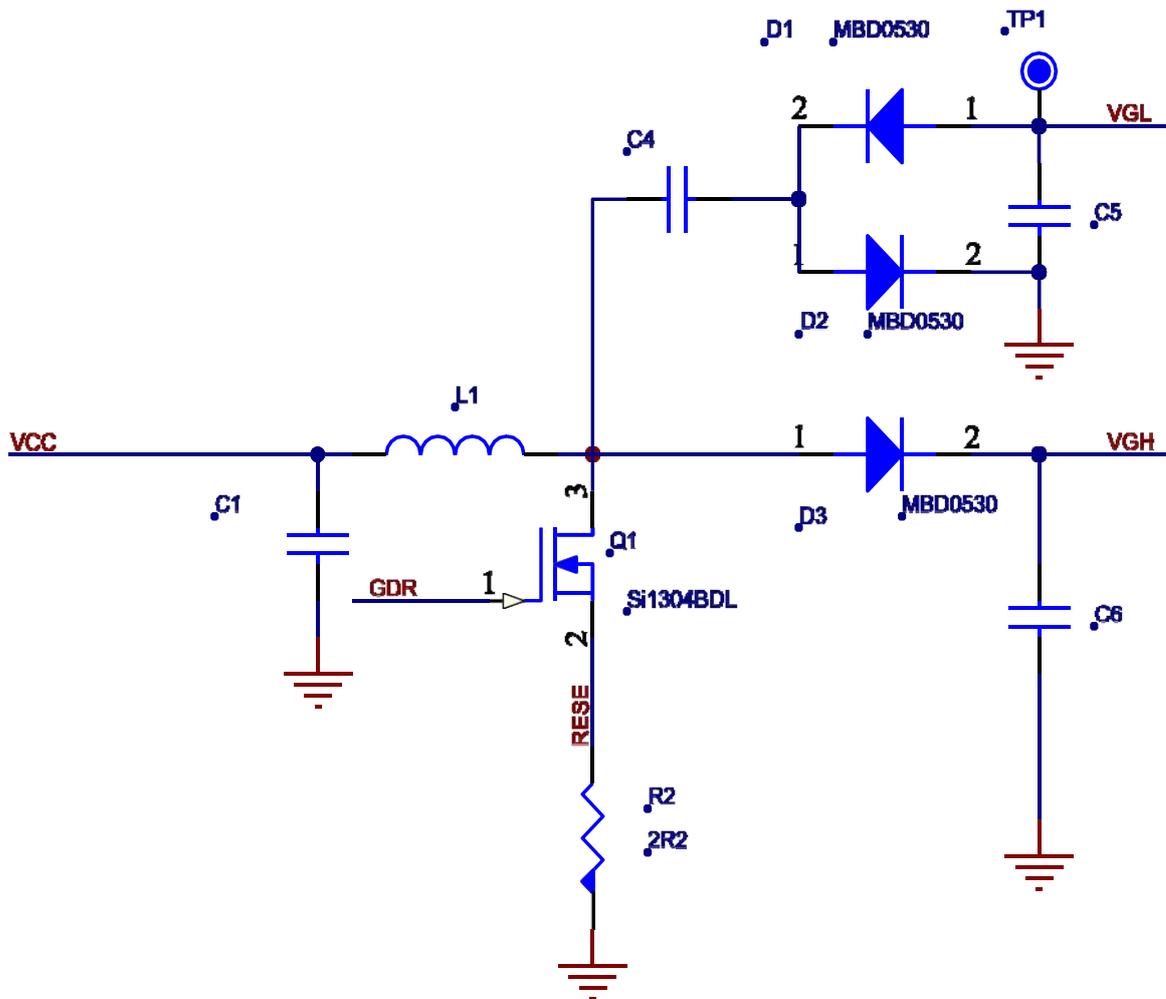
Part Name	Value/Type	Requirement/Reference Part
C1—C3	1uF	0603; X5R/X7R; Voltage Rating: 6V
C4-C9	4.7uF	0805; X5R/X7R; Voltage Rating: 25V
C10	1uF	0805; X7R; Voltage Rating: 25V
D1—D3	Diode	MBR0530 1) Reverse DC voltage≥30V 2) Io≥500mA 3) Forward voltage≤430mV
R2	2.2 Ω	0805：1% variation
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage≥30V 2) Vgs（th）=0.9（Typ），1.3V（Max） 3) Rds on≤ 2.1Ω& Vgs=2.5V
L1	47uH	CDRH2D18/LDNP-470NC Io=500（Max）
CON24Pin	0.5mm ZIF Socket	24Pins,0.5mm pitch

10. ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V$_{CI}$	Logic supply voltage	-0.5 to +6.0	V	-	-	
T$_{OPR}$	Operation temperature range	0 to 40	°C	45 to70	%	Note 10-1
Tttg	Transportation temperature range	-25 to 60	°C	45 to70	%	Note10-2
Tstg	Storage condition	0 to 40	°C	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to70	%	

Note 10-1：We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note10-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃or 40℃~60℃.

Note 10-3：When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months. We suggest that the full black and full white picture could be added to clear the screen after the module is refreshed for a long time, the display effect would be better.

11. DC CHARACTERISTICS

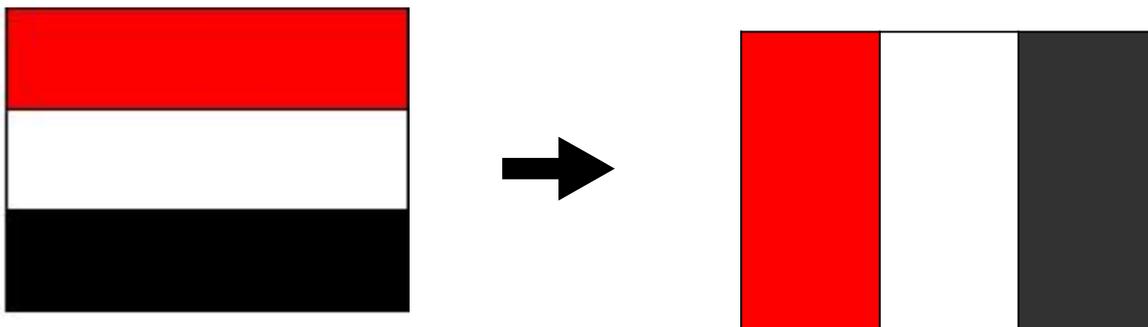The following specifications apply for: VSS=0V, VCI=3.3V, T$_{OPR}$=25℃.

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicabl pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.5	3.3	3.7	V
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#,RES#, BS1	0.8VDDIO	-	-	V
VIL	Low level input voltage	-		-	-	0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY,	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA		-	-	0.1VDDIO	V
Iupdate	Module operating current	-	-	-	15	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	-	7	uA

- The Typical power consumption is measured using associated 25℃ waveform with followingpattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller &waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption

12. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.5V to 3.7V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CSB has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CSB has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

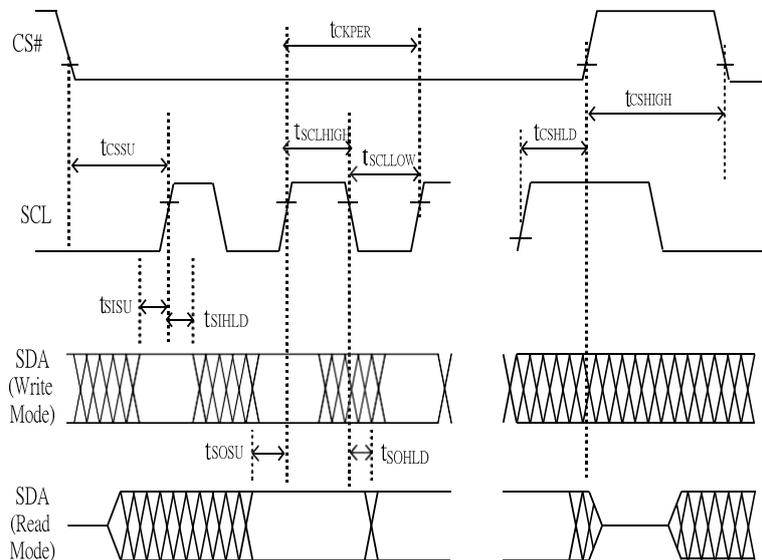Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 13-1: Serial peripheral interface characteristics

13. Power Consumption

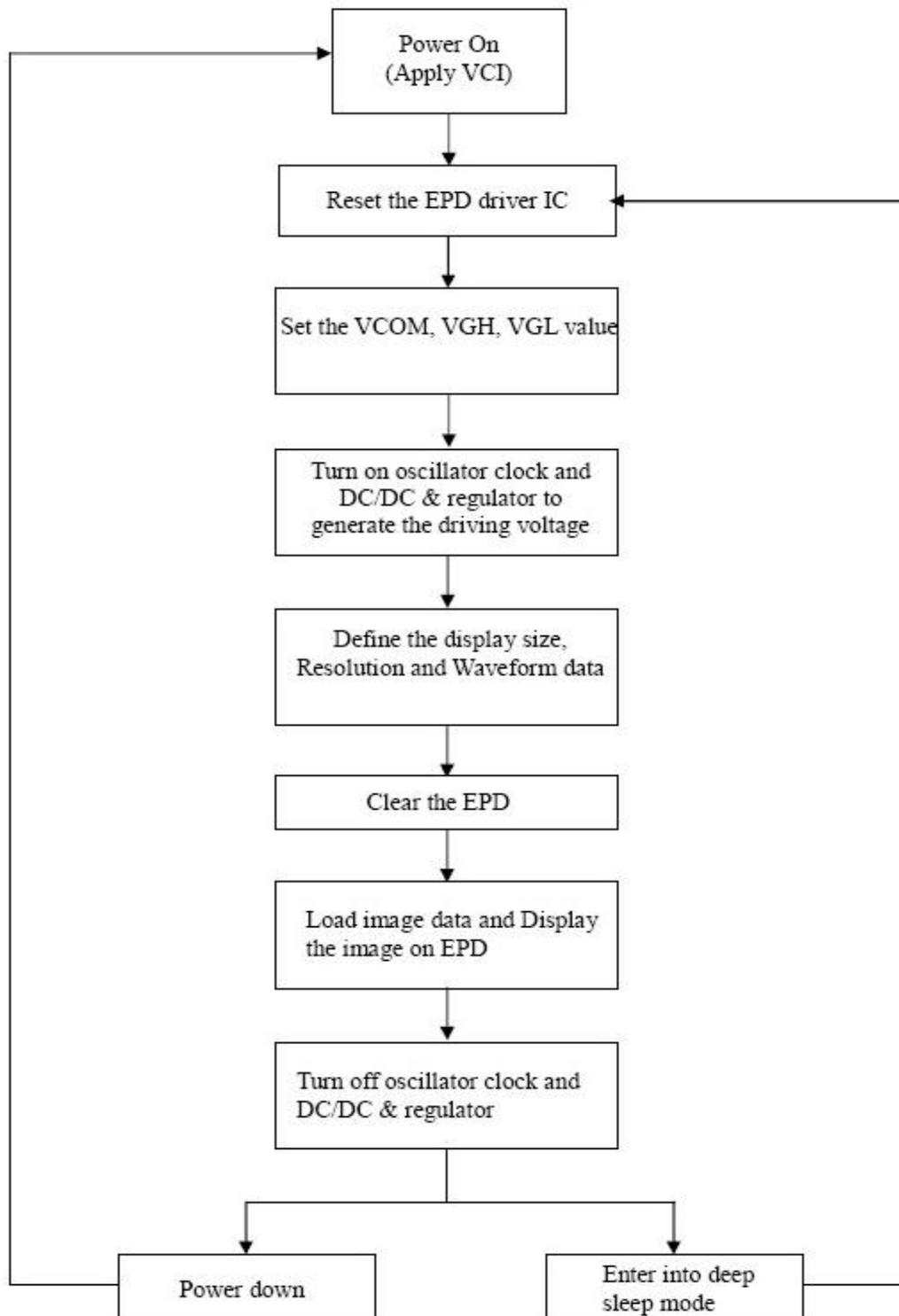| Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	400	mAs	-
Deep sleep mode	-	25℃	-	7	uA	-

Mas=update average current × update time

14. Typical Operating Sequence

14.1 Normal Operation Flow

```
                    ┌─────────────────────┐
              ┌────>│     Power On         │
              │     │    (Apply VCI)       │
              │     └──────────┬──────────┘
              │                │
              │                ▼
              │     ┌─────────────────────┐
              │     │ Reset the EPD driver IC│<────────┐
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │ Set the VCOM, VGH, VGL value │    │
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │ Turn on oscillator clock and │    │
              │     │   DC/DC & regulator to       │    │
              │     │ generate the driving voltage │    │
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │ Define the display size, │        │
              │     │ Resolution and Waveform data │    │
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │    Clear the EPD     │            │
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │ Load image data and Display │     │
              │     │    the image on EPD  │            │
              │     └──────────┬──────────┘           │
              │                │                        │
              │                ▼                        │
              │     ┌─────────────────────┐            │
              │     │ Turn off oscillator clock and │   │
              │     │   DC/DC & regulator  │            │
              │     └──────────┬──────────┘           │
              │         ┌──────┴──────┐                 │
              │         ▼             ▼                 │
              │  ┌───────────┐  ┌──────────────┐       │
              └──│ Power down│  │ Enter into deep │─────┘
                 └───────────┘  │  sleep mode    │
                                └──────────────┘
```

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14.2 Reference Program Code

```
Power On
(Apply VCI)
        │
        ▼
Init all the pin
D/C#,CS#,SDA,SCL,
RES# to high level,
```

BS1 High   BS1 Low

```
3-wire spi              4-wire spi
communication mode      communication mode
```

```
Panel Reset
RES# =LOW 10ms
RES#=HIGH 10ms
Software Reset
SPI(0x12)
```

```
Init Code:
SPI(0x74,0x54)
SPI(0x7E,0x3B)
SPI(0x01,0x7F,0x02,0x00)
```

```
Dara entry sequence setting (Y+,X-)
SPI(0x11,0x01)
```

```
Set RAMX Start/end position
SPI(0x44,0x00,0x00,0xBF,0x03)
Set RAMY Start/end position
SPI(0x45, 0x7F,0x02,0x00,0x00)
```

```
Detect Temperature, Convert into value
SPI(0x1A, value)
Display update sequence setting: Load
LUT from OTP
SPI(0x22, 0x91)
Master Activation:
```

Busy → Busy High

Busy Low

```
Set RAMX address counter
SPI(0x4e,0x00)
Set RAMY address counter
SPI(0x4f, 0x7F,0x02)
Write BW RAM
SPI(0x24,76800 byte data)
Set RAMX address counter
SPI(0x4e,0x00)
Set RAMY address counter
SPI(0x4f,0x7F,0x02)
Write Red RAM
SPI(0x26, 76800 byte data)
```

```
Display update sequence setting: Start
Display
SPI(0x22, 0xC7)
Master Activation:
```

Busy → Busy High

Busy Low

```
Enter Deepsleep
SPI(0x10,0x01)
```

15. Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unlessotherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
KS	Black State L* value		-	13	14		Note 15-1
	Black State a* value		-	3	4		Note 15-1
WS	White State L* value		63	65	-		Note 15-1
RS	Red State L* value	Red	25	28	-		Note 15-1
	Red State a* value	Red	36	40	-		Note 15-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state , RS: Red state
Note 15-1 : Luminance meter : i - One Pro Spectrophotometer

15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area(Rd)() :

R1: white reflectance   Rd: dark reflectanceCR = R1/Rd
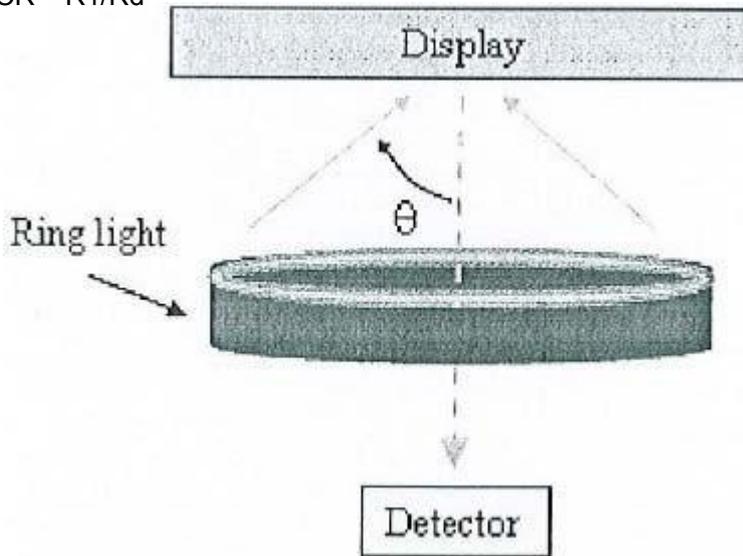
15.3 Reflection Ratio

The reflection ratio is expressed as :

$R = $ Reflectance Factor $_{white\,board}$ x (L_{center} / $L_{white\,board}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1) . $L_{white\,board}$ is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .
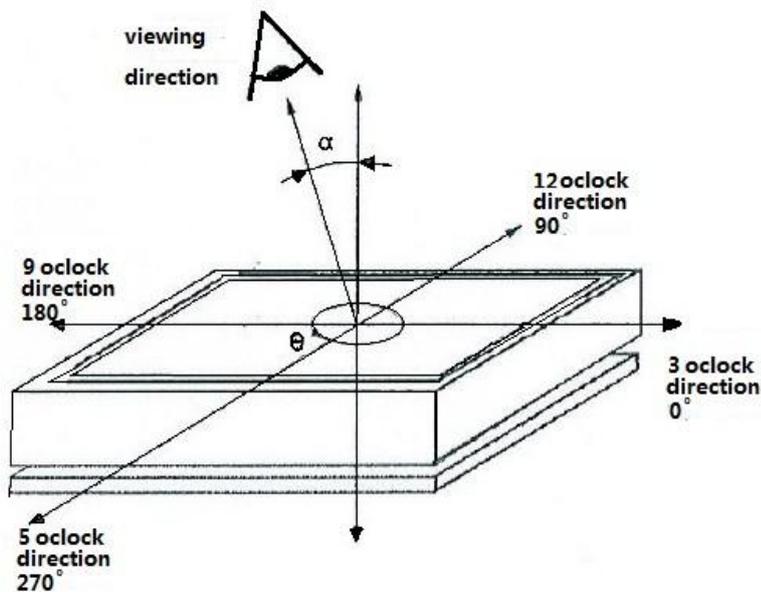
16. HANDLING,SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along thelong axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and frontsurfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied tothe module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD.Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generatescorrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please donot rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Somecosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soakswith petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and colorfading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specificationsis not warranted after any Post-assembled operation.

17. Reliability test
17.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=50℃RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃，RH=90%RH，For 168Hr	
6	High Temperature, High-Humidity Storage	T=50℃，RH=80%RH，For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min)，50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200HzDirection : X,Y,Z Duration: 30minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100cm onConcrete surface Drop sequence:1 corner, 3edges,6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before

temperature test.Note2：Stay white pattern for storage and

non-operation test.

Note3：Operation is black/white/red pattern , hold time is 150S.

Note4：The function, appearance ,opticals should meet the requirements of the test before and after the

test. Note5：Keep testing after 2 hours placing at 20℃-25℃.

17.2 Product life time

The EPD Module is designed for a 5-year life-time with 25 ℃/60%RH operation assumption. Reliability estimation testingwith accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.
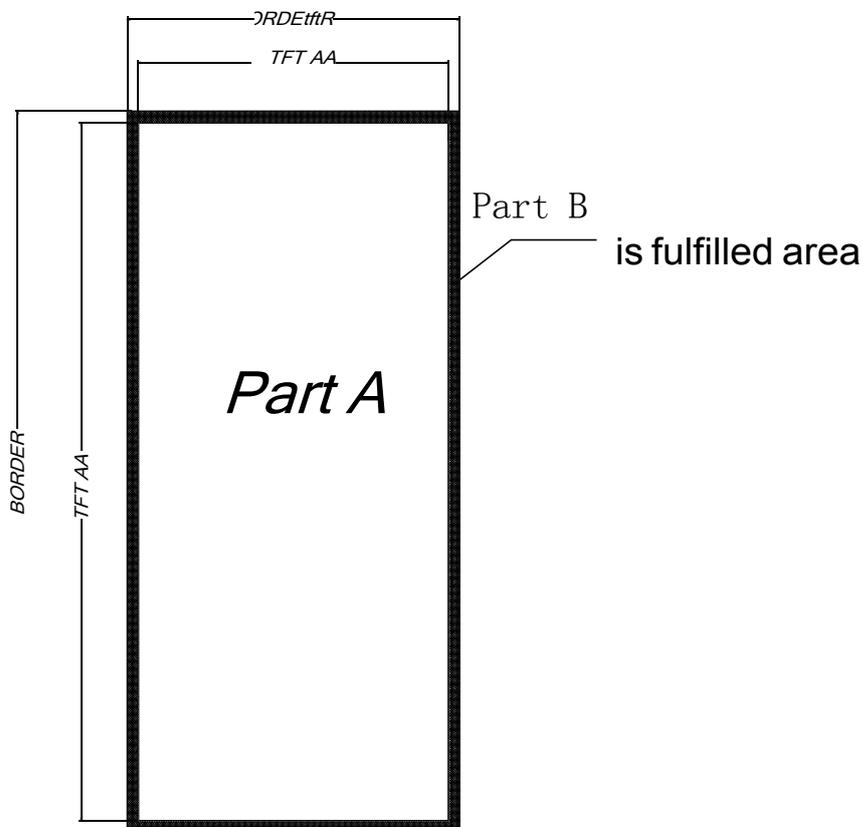
17.3 Product warranty

Warranty conditions have to be negotiated between SID and individual customers.
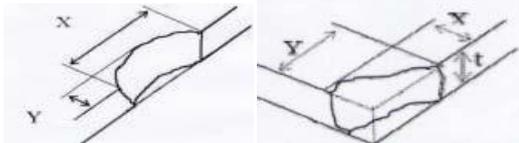SID provides 12+1(one month delivery time) months warranty for all products which are purchased from SID.

18. Block Diagram
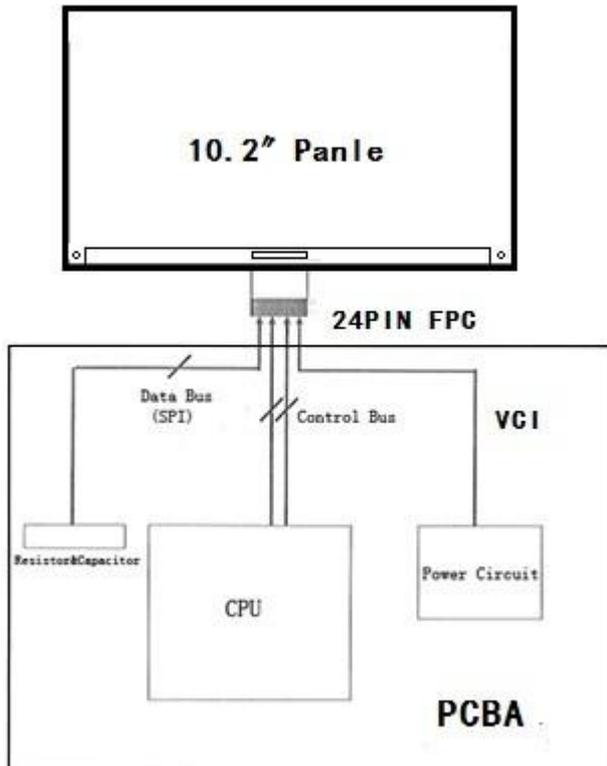
19. PartA/PartB specification

20 Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	224(H)×157(V)×0.9(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.4 ㎜		Ignore		Ignore
		0.4 ㎜＜D≤0.6 ㎜		N≤4		Ignore
		0.6 ㎜＜D≤0.8 ㎜		N≤1		Ignore
		D＞0.8 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.1 ㎜		Ignore		Ignore
		2mm＜L≤9.0mm，0.1＜W≤0.2mm,		N≤2		Ignore
		L＞9.0 ㎜，W＞0.2 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.4mm		Ignore		Ignore
		0.4mm≤D≤0.6mm		N≤4		Ignore
		D＞0.6 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	Do not affect the electrode circuit((Corner chipping) X≤8mm，Y≤1mm, Do not affect the electrode circuit, Ignore				
Warp	Plug gauge	t≤5mm,OK				
Remark	1. Appearance defect should not cause electrical defects					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					

L1

W

L2

L = L1 + L2

Line Defect

L

W
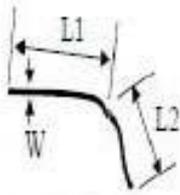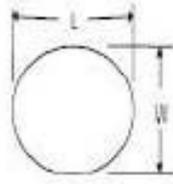
D = (L + W)/2

Spot Defect

L=long   W=wide D=point size

21 Packing

TBD