o Tentative Specification
✓ Preliminary Specification
o Specification Approval

Specification For SID 4.20” BWR EPD

Model Name: JS0420MN11-TNG-A0

Version: V0.1

SID	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE	JY. Guo	Z.Nong	RJ. Wu
DATE	20220905	20220905	20220905

CUSTOMER APPROVAL	SIGNATURE	DATE
	Notes:	

Notes :

1、Please contact SID before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	2022.09.05	First release	Preliminary

CONTENTS

1. General Description

SE0420MN11-A0 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design.The4.2”active area contains 400×300 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 400×300 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

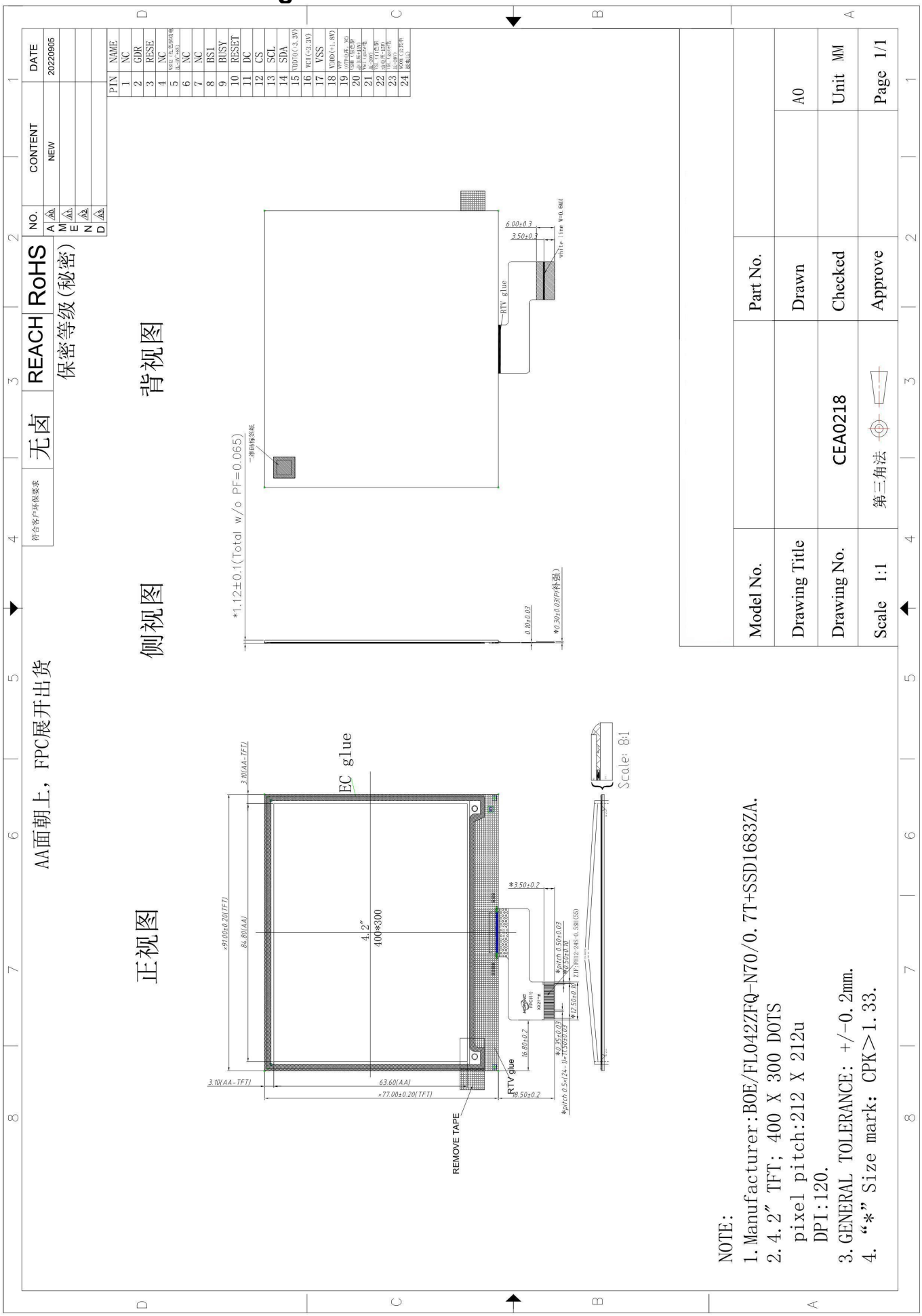
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:120
Active Area	84.8(H)×63.6(V)	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Rectangle		
Outline Dimension	**91.0(H)×77.0 (V) ×1.12(D)**	mm	**Without masking film**
Weight	15.5±0.5	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	NC	No connection and do not connect with other NC pins	Keep Open
7	NC	No connection and do not connect with other NC pins	Keep Open
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset signal input.	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	The chip select input connecting to the MCU.	Note 6-1
13	SCL	Serial clock pin for interface.	
14	SDA	Serial data pin for interface.	
15	VDDIO	Power input pin for the Interface.	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground (Digital)	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip isenabled forMCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When thepin ispulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High ,the operation of chipshouldnot be interrupted and any commands should not be issued to the module. The driver IC will put Busypin High when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI isselected.When it is “High”, 3-line SPI (9 bits SPI) is selected

7. MCU Interface

7.1 MCU interface selection

The MOFANG-M006F can support 3-wire/4-wire serial peripheral interface. In the Module,theMCU interface is pin selectable by BS1 pins shown in.

Table 7-1: MCU interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wireSPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Figue 7-2.

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Table 7-2 : Control pins status of 4-wire SPI

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order ofD7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

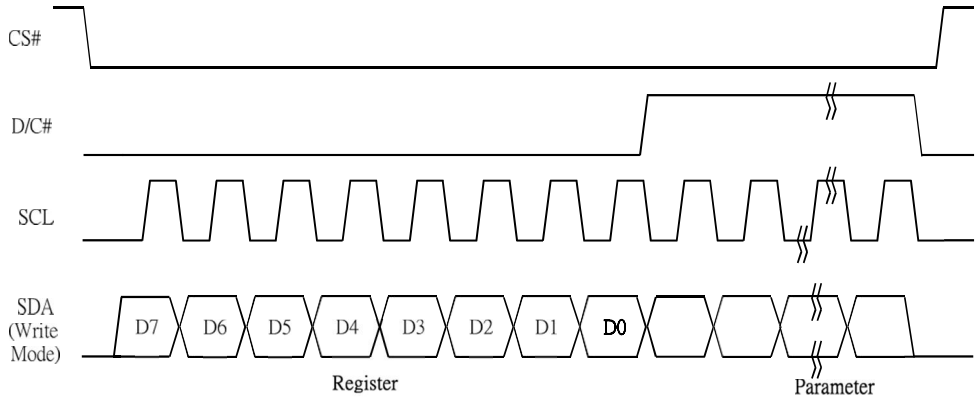


Figure 7-1: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7,D6, ...D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, …D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS#needto drive to high to stop the read operation.

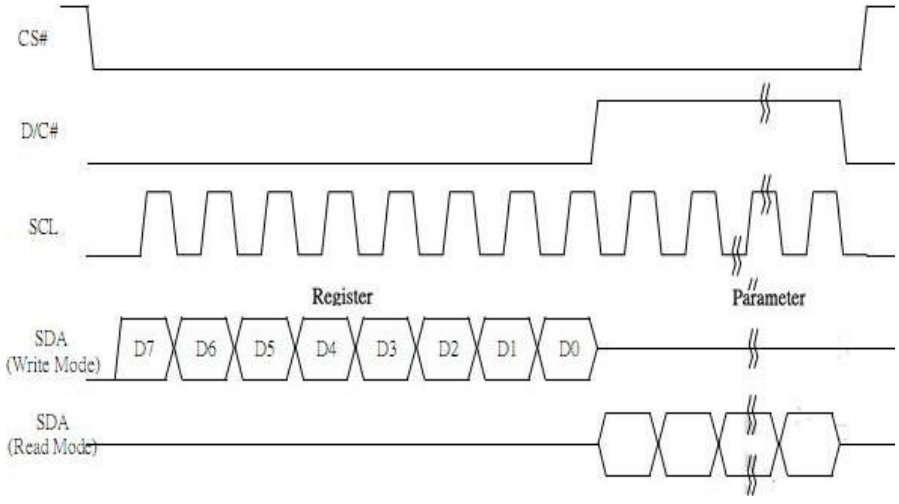


Figure 7-2: Read procedure in 4-wire SPI mode

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order ofD7, D6, ...D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wireSPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bitshifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bitis 1, the following byte is data. shows the write procedure in 3-wire SPI

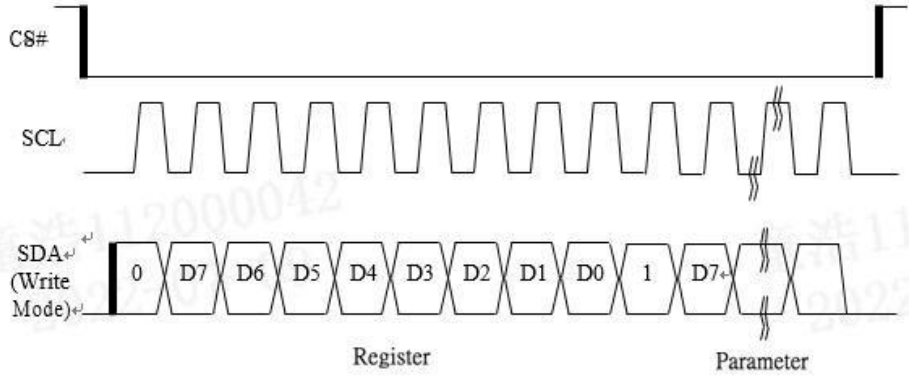


Figure 7-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C#=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7,D6, ...D0.
4. D/C#=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, …D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read,CS# needto drive to high to stop the read operation.

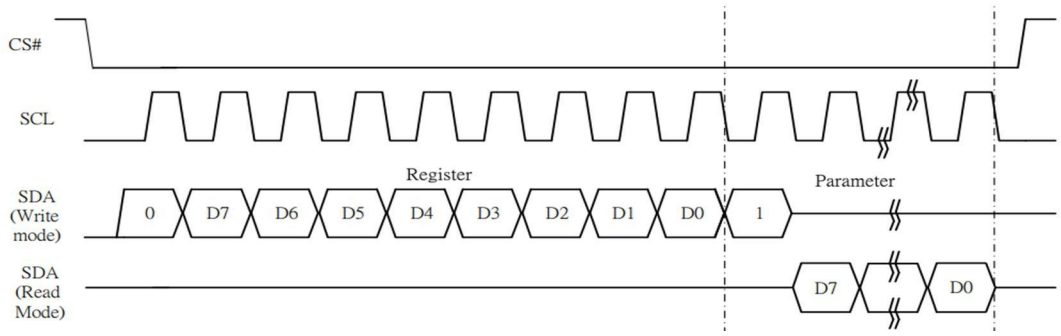


Figure 7-4: Read procedure in 3-wire SPI mode

8. Reference Circuit

Figure 13-1: Schematic of SSD application circuit

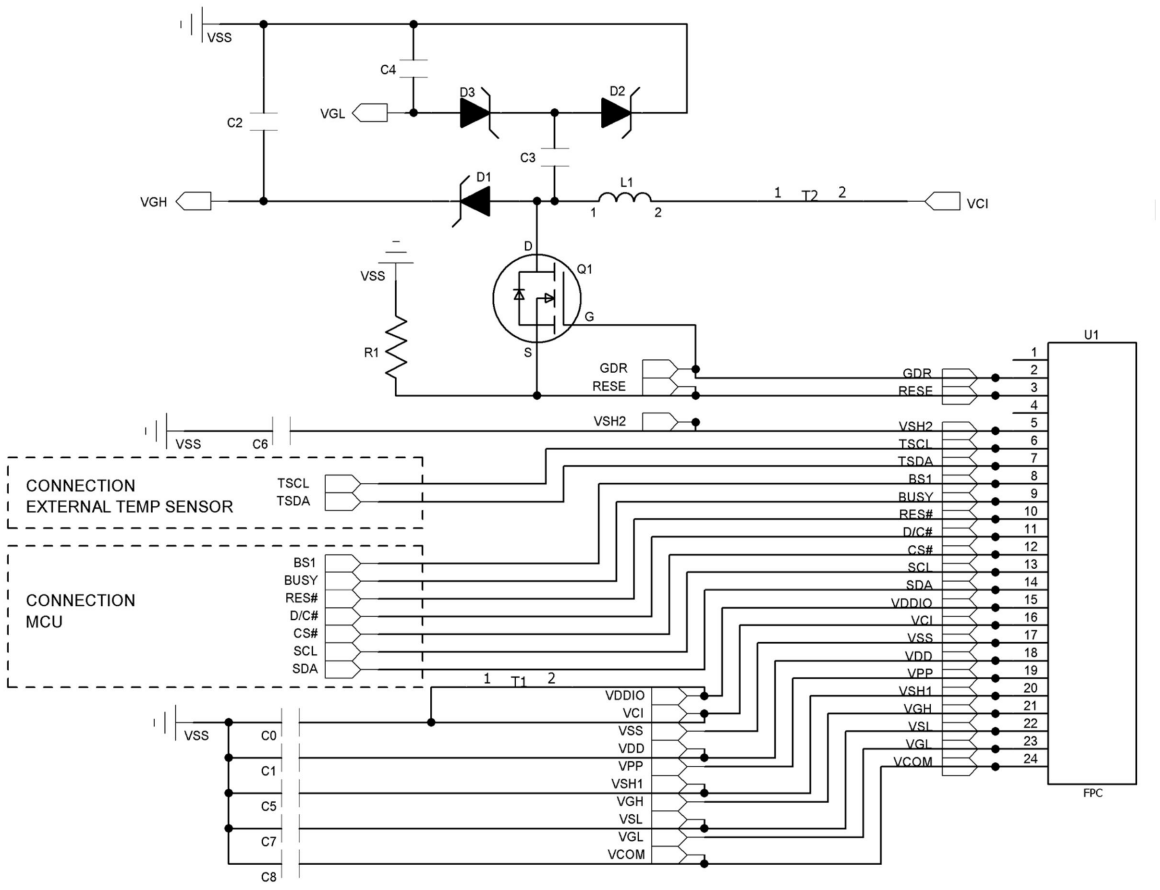


Table 13-1: Component list for SSD application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0603/0805; X7R; Voltage Rating : 25V Note: Effective capacitance > 0.25uF @ 18V DC bias
R1	2.2 ohm	0402, 0603, 0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remarks:

1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

9. Absolute Maximum Rating

Table 9-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 40	°C	35 to70	%	Note 9-1
Tttg	Transportation temperature range	-25 to 60	°C	35 to70	%	Note 9-2
Tstg	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	35 to70	%	

Note 9-1：We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note 9-2: Tttg is the transportation condition,the transport time is within 10 days for -25℃~0℃or 40℃~60℃.

Note 9-3：When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months.

10. DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25℃.

Table 13-1: DC Characteristics

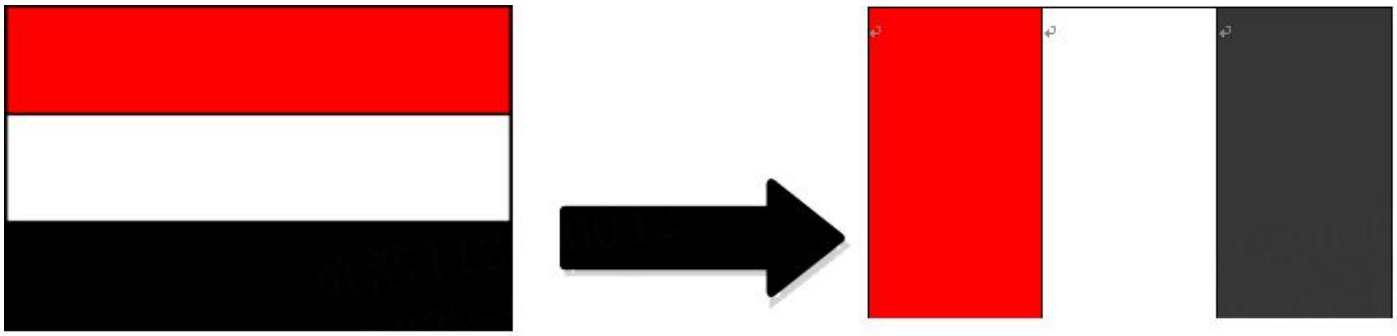
Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.3	3	3.7	V
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#,BS1	0.8VDDIO			V
VIL	Low level input voltage	-		-	-	0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA		-	-	0.1VDDIO	V
Iupdate	Module operating current	-	-	-	6	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	-	3	uA

The Typical power consumption is measured using associated 25℃ waveform withfollowingpattern transition: from horizontal scan pattern to vertical scan pattern. (Note10-1)

- The listed electrical/optical characteristics are only guaranteed under thecontroller &waveform provided by MoFang.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 10-1

The Typical power consumption



11. Serial Peripheral Interface Timing and Command Table

11.1 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.3V to 3.7V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

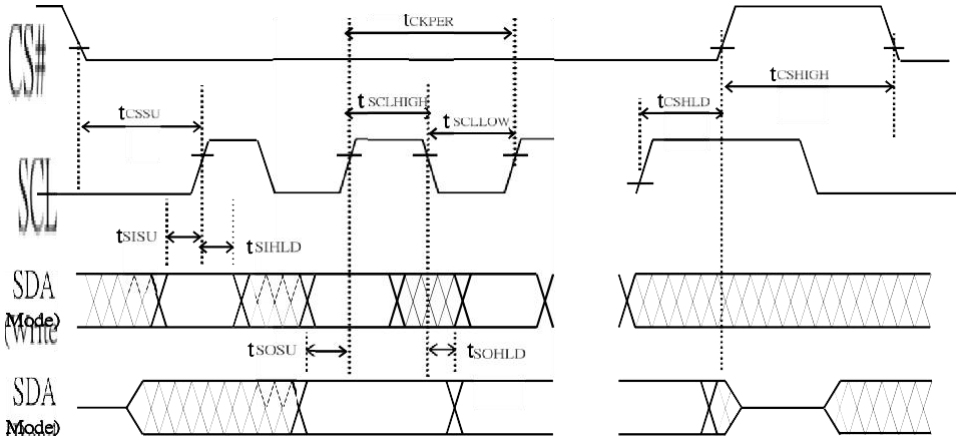


Figure 11-1: SPI timing diagram

11.2 Command Table

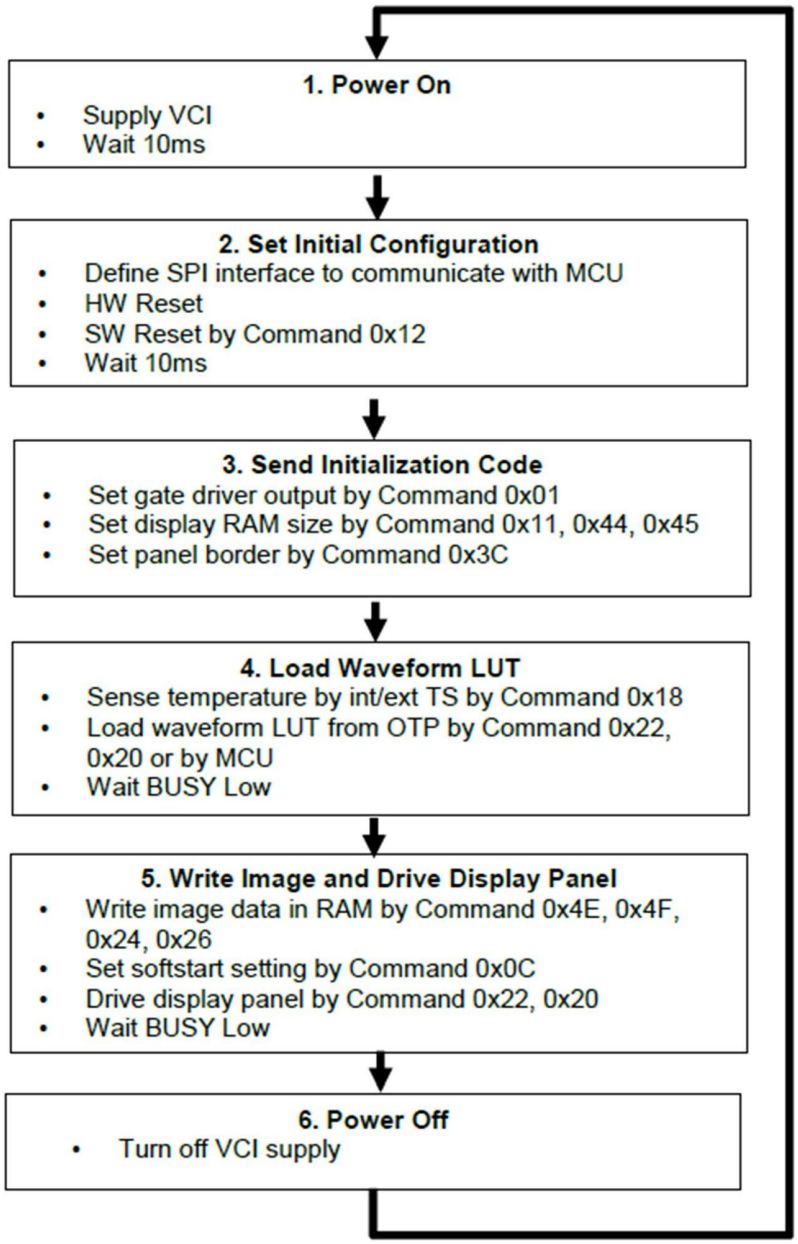
Please refer to IC Spec.

12. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	180	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

mAs=update average current ×update time

13. Typical Operating Sequence



14. Optical characteristics

14.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 14-1
CR	Contrast Ratio	-	15	20	-		-
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
KS	Black State L* value		-	-	14		Note 14-1
	Black State a* value		-	-	6		Note 14-1
WS	White State L* value		63	65	-		Note 14-1
RS	Red State L* value	Red	25	28	-		Note 14-1
	Red State a* value	Red	36	40	-		Note 14-1
Panel's life	-	0℃～40℃		5years	-	-	Note 14-2
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state, RS: Red state

Note 14-1 : Luminance meter : i - One Pro Spectrophotometer

Note 14-2:We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH; Suggest Updated once a day;

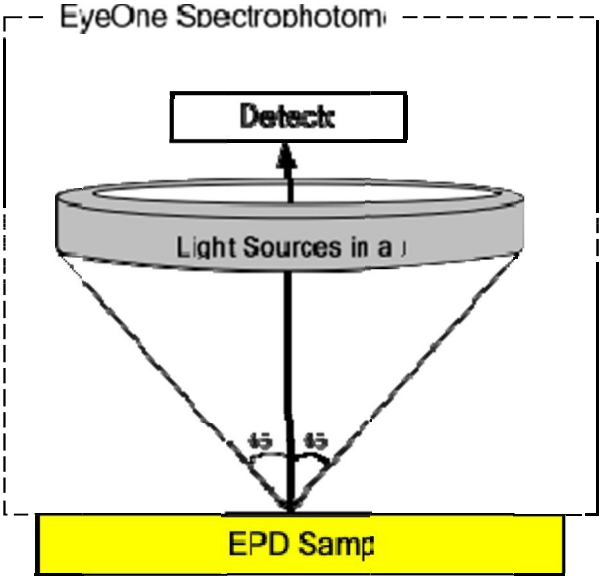
Note 14-3: To increases the black and white screen clear screen when red has refreshed for a long time , the effect is better。

Note: It's only with the 25℃ and 51% RH for 5 years.

14.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectanceCR = R1/Rd

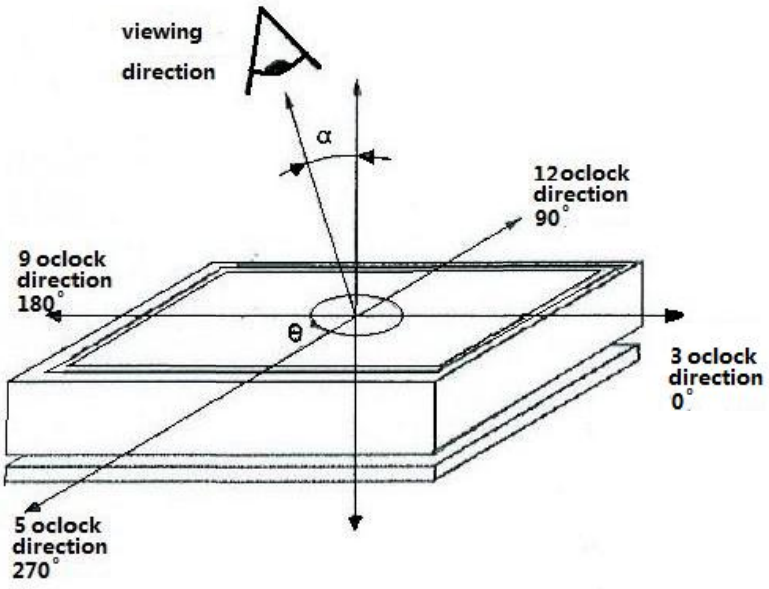


14.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard whiteboard. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



15. Handling, Safety and Enviromental Requirements

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along thelong axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD.Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generatescorrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please donot rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Somecosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soakswith petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and colorfading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

16. Reliability test

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=50℃,RH=30%RH,For 240Hr	
2	Low-Temperature Operation	T = 0℃for 240 Hr	
3	High-Temperature Storage	T=60℃RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃for 240 Hr	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH,For 168Hr	
6	High Temperature, High-Humidity Storage	T=60℃,RH=80%RH,For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min),50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200HzDirection : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm onConcrete surface Drop sequence:1 corner, 3edges,6face One drop for each.	Full packed for shipment
10	Electrostatic discharge	HBM:330Ω,150pF	Air +/-4KV;Contact +/-2KV
11	UV Exposure Resistance	765 W/ ㎡for 168hrs,40 ℃	

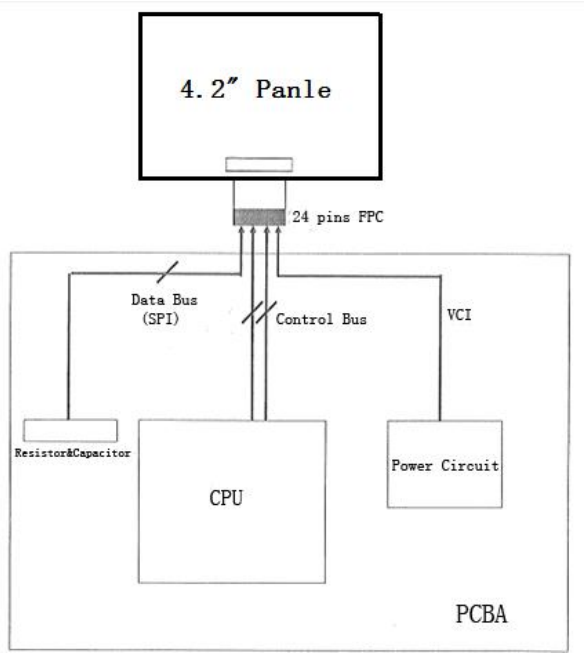
Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

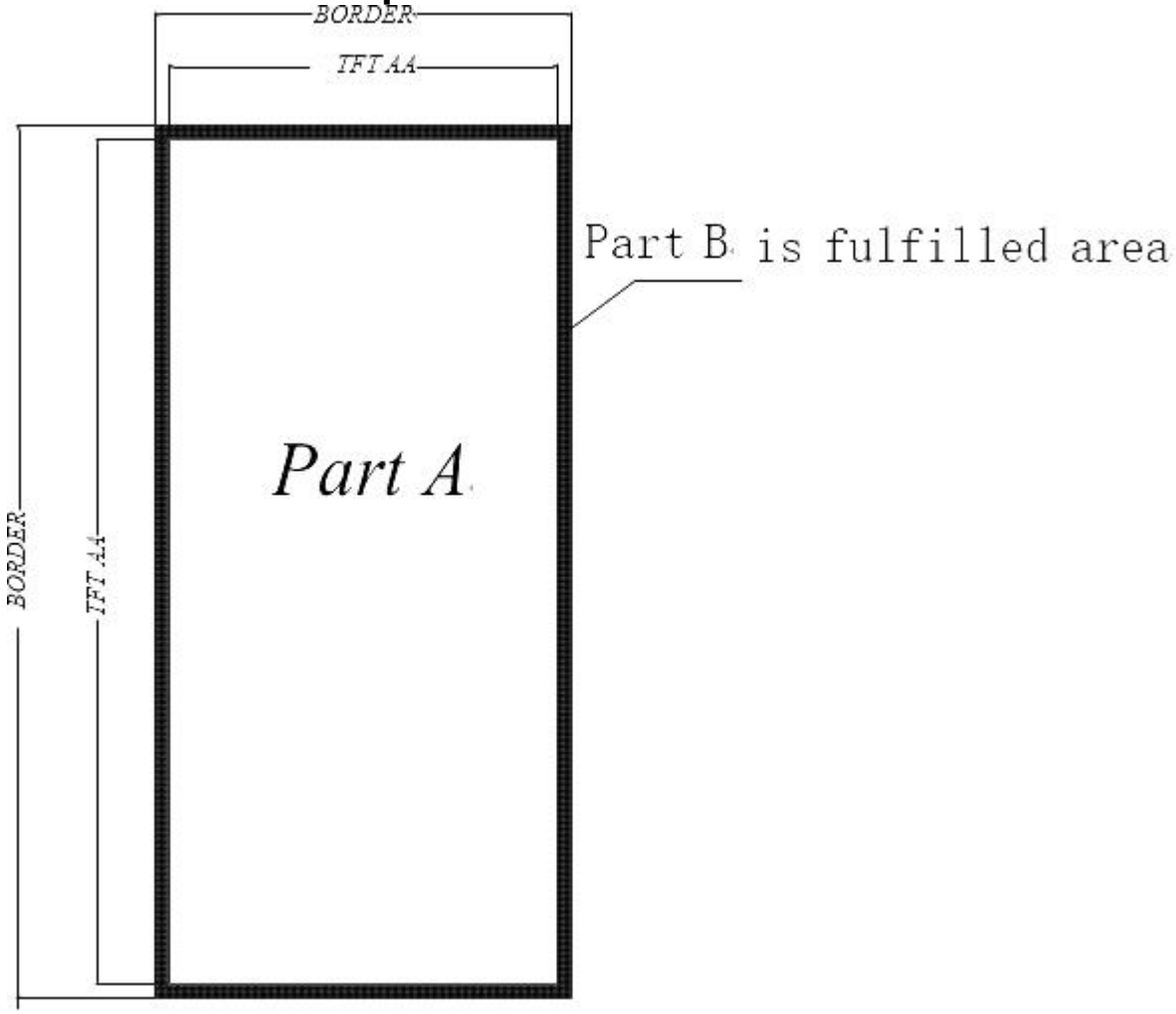
Note2：Operation is black/white/red pattern , hold time is 150S.

Note3：The function ,appearance, opticals should meet the requirements of the test before and after the test. Note4: Keep testing after 2 hours placing at 20℃-25℃

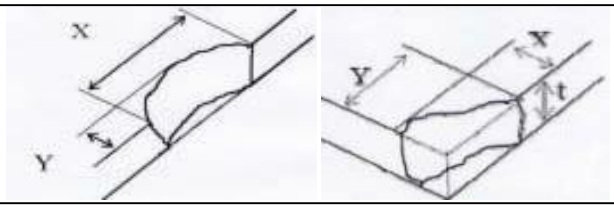
17. Block Diagram



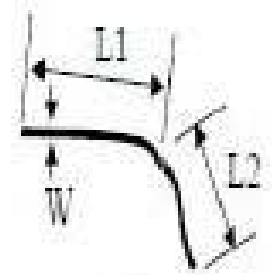
18. PartA/PartB Specification



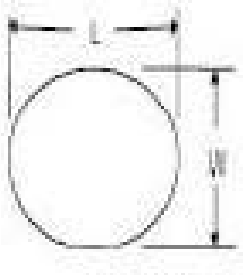
19. Point and line standard

<table>
<tr><th colspan="8">Shipment Inspection
Standard</th></tr>
<tr><td colspan="8">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>91(H)×77(V)×1.12(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td colspan="2">Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td colspan="2">Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5% RH</td><td>600～1200Lux</td><td>300 ㎜</td><td>35Sec</td><td colspan="2"></td></tr>
<tr><td>Defect type</td><td>Inspection method</td><td colspan="3">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">Electric Display</td><td colspan="3">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">0.25 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="3">D＞0.4 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="3">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="3">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="3">L≤2 ㎜,W≤0.2 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">2.0mm＜L≤5.0mm,0.2＜W≤0.3mm,</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="3">L＞5 ㎜,W＞0.3 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="3">D≤0.2mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="3">0.2mm≤D≤0.35mm & N≤4</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="3">D＞0.35 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping)
Ignore</td></tr>
<tr><td colspan="5"> 
</td></tr>
</table>

Remark	1.Cannot be defect & failure cause by appearance defect；
	2.Cannot be larger size cause by appearance defect；
	L=long W=wide D=point size N=Defects NO



Line Defect



Spot Defect

L=long **W=wide** **D=point size**

20. Barcode

TBD

21. Packing

TBD