



- Tentative Specification
- ☒ Preliminary Specification
- Specification Approval

Specification For SID 2.90” BW EPD

Model Name: JS0290NQ20-MNG-A0

Version:V0.1

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	Notes:	

Notes :

- 1、 Please contact SID before assigning your product based on this module specification.
- 2、 To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

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1 General Description

SE0290NQ20-NNG-A0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 2.90 inches active area contains 128×296 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 128X296 pixels display
- ◆ High contrast
- ◆ High reflectance
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor

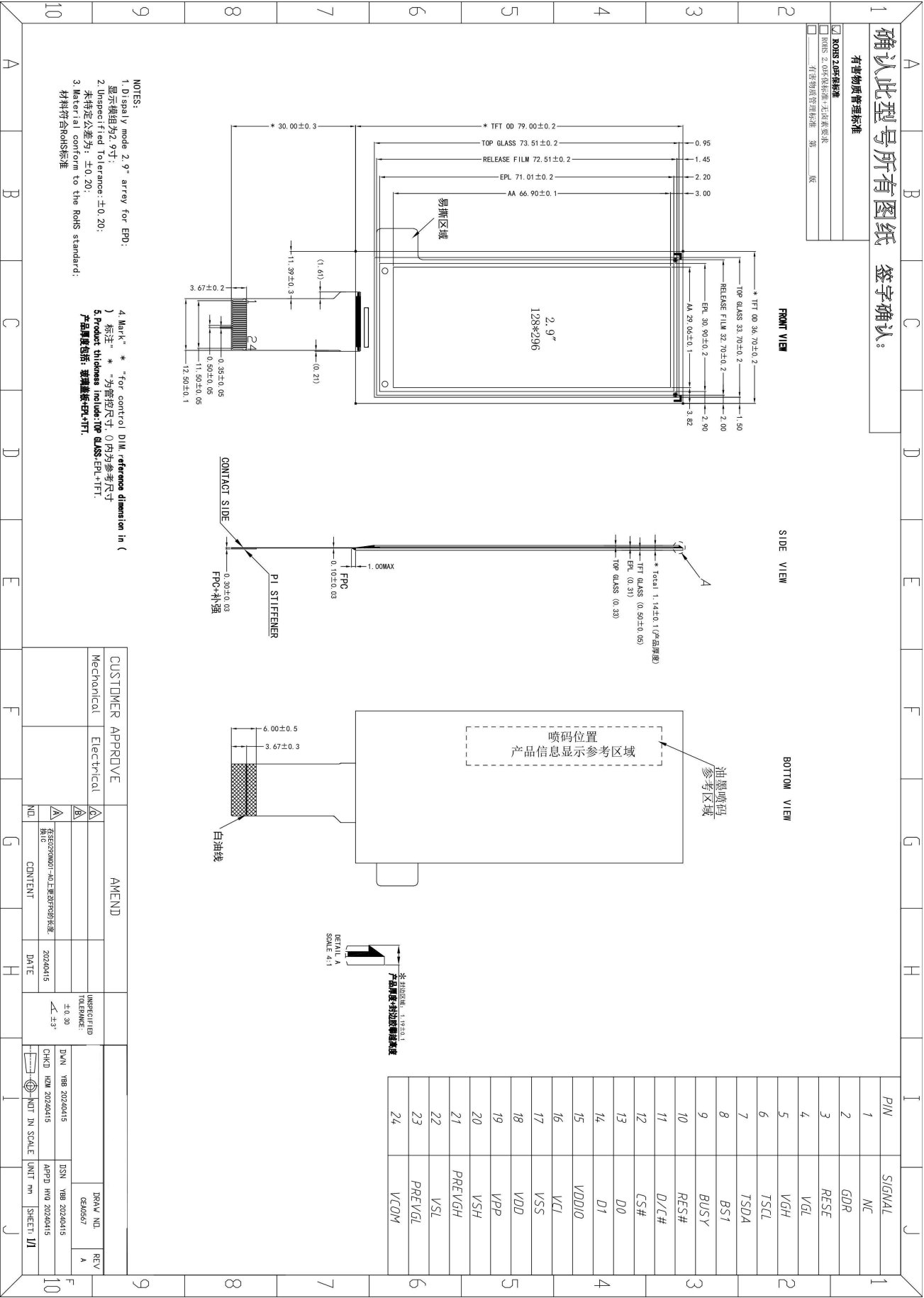
3 Application

Electronic Shelf Label System

4 Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.90	Inch	
Display Resolution	128(H)×296(V)	Pixel	
Active Area	29.06(H)×66.90(V)	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.70(H)×79.00(V) ×1.14(D)	mm	
Weight	TBD	g	

5 Mechanical Drawing of EPD module



6 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 6-5
9	BUSY	O	Busy state output pin	Note 6-4
10	RES#	I	Reset signal input. Active Low.	Note 6-3
11	D/C#	I	Data /Command control pin	Note 6-2
12	CS#	I	Chip select input pin	Note 6-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 6-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputtingdisplay waveform - Communicating with digital temperature sensor

Note 6-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V _{CI}	-0.5 to +4.0	V
Logic Input voltage	V _{IN}	-0.5 to V _{CI} +0.5	V
Logic Output voltage	V _{OUT}	-0.5 to V _{CI} +0.5	V

Note:

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

7.2 Panel DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =25°C.

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	V _{CI}	2.2	3.0	3.6	V
High level input voltage	V _{IH}	-	-	0.8 V _{CI}	-	V _{CI}	V
Low level input voltage	V _{IL}	-	-	-	-	0.1 V _{CI}	V
High level output voltage	V _{OH}	I _{OH} = -100uA	-	0.9V _{CI}	-	-	V
Low level output voltage	V _{OL}	I _{OL} = 100uA	-	-	-	0.1 V _{CI}	V
Typical operating current	I _{opr} _V _{CI}	V _{CI} =3.0V	-	-	4	-	mA
Deep sleep mode current	I _{dslp} _V _{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	-	uA

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

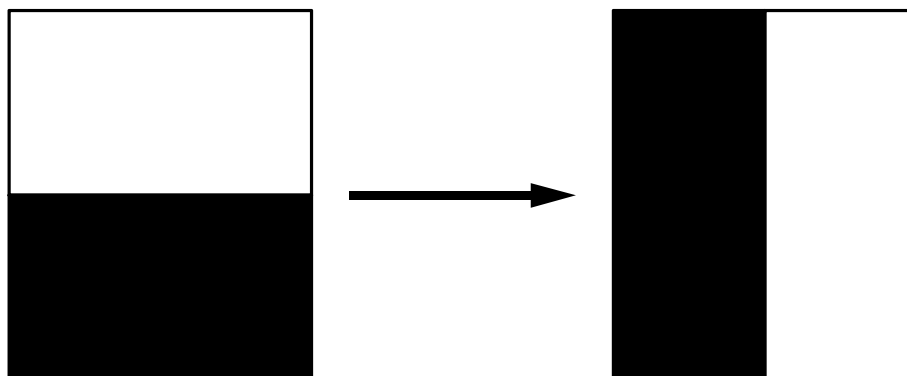


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

7.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR}=25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-3.0	-	-0.2	V

7.4 Panel AC Characteristics

7.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 7-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 7-4-1: MCU interface assignment under different bus interface mode

7.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 7-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

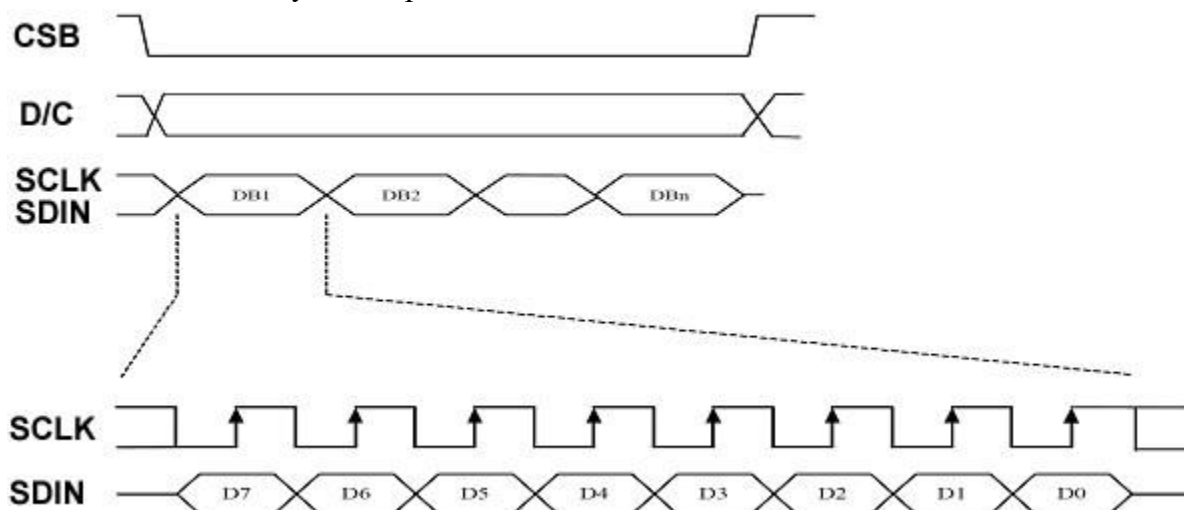


Figure 7-4-2: Write procedure in 4-wire SPI mode

7.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/Cbit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Table 7-4-3: Control pins of 3-wire Serial interface

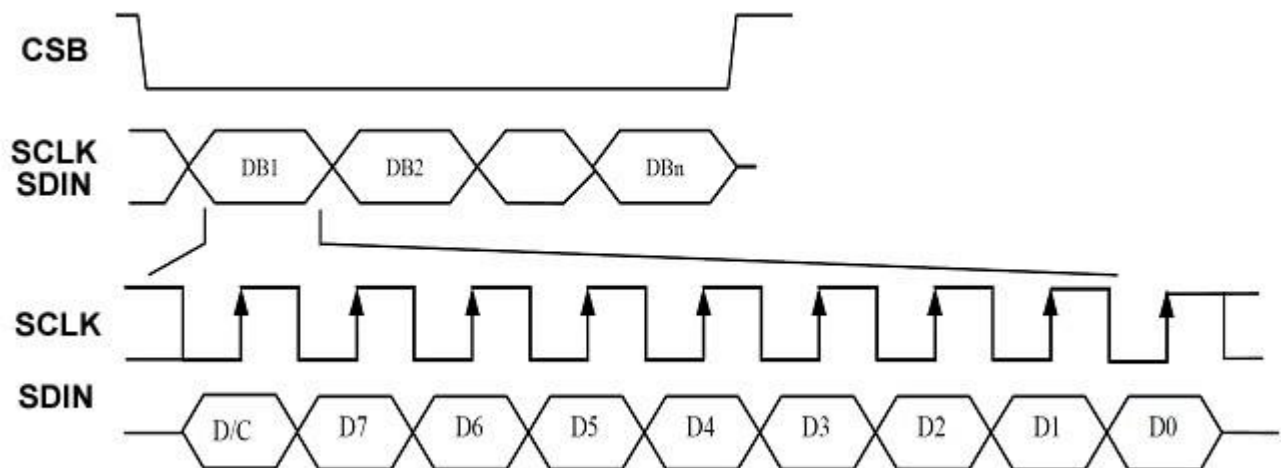


Figure 7-4-3: Write procedure in 3-wire SPI mode

7.4.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, TOPR =25°C.

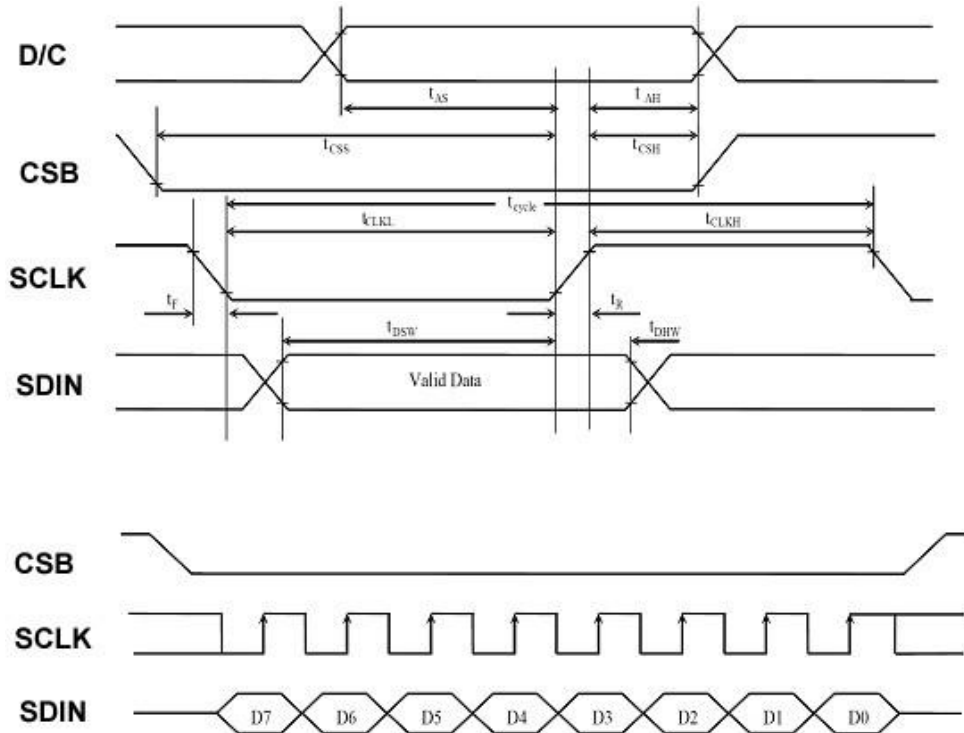


Figure 7-4-4: Serial interface characteristics

(Vdd - VSS = 2.4V to 3.3V, TOPR = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t _{cycle}	Clock Cycle Time	250	-	-	ns
t _{AS}	Address Setup Time	150	-	-	ns
t _{AH}	Address Hold Time	150	-	-	ns
t _{CSS}	Chip Select Setup Time	120	-	-	ns
t _{CSH}	Chip Select Hold Time	60	-	-	ns
t _{DSW}	Write Data Setup Time	50	-	-	ns
t _{DHW}	Write Data Hold Time	15	-	-	ns
t _{CLKL}	Clock Low Time	100	-	-	ns
t _{CLKH}	Clock High Time	100	-	-	ns
t _R	Rise Time [20% ~ 80%]	-	-	15	ns
t _F	Fall Time [20% ~80%]	-	-	15	ns

Table 7-4-4: Serial Interface Timing Characteristics

8 Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
White Δ L 24h	Reduce		-	≤ 4	-	-	-
Tupdate(5S)	Image update time	at 25 °C	-	3300	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9 Handling,Safety and Enviromental Requirements

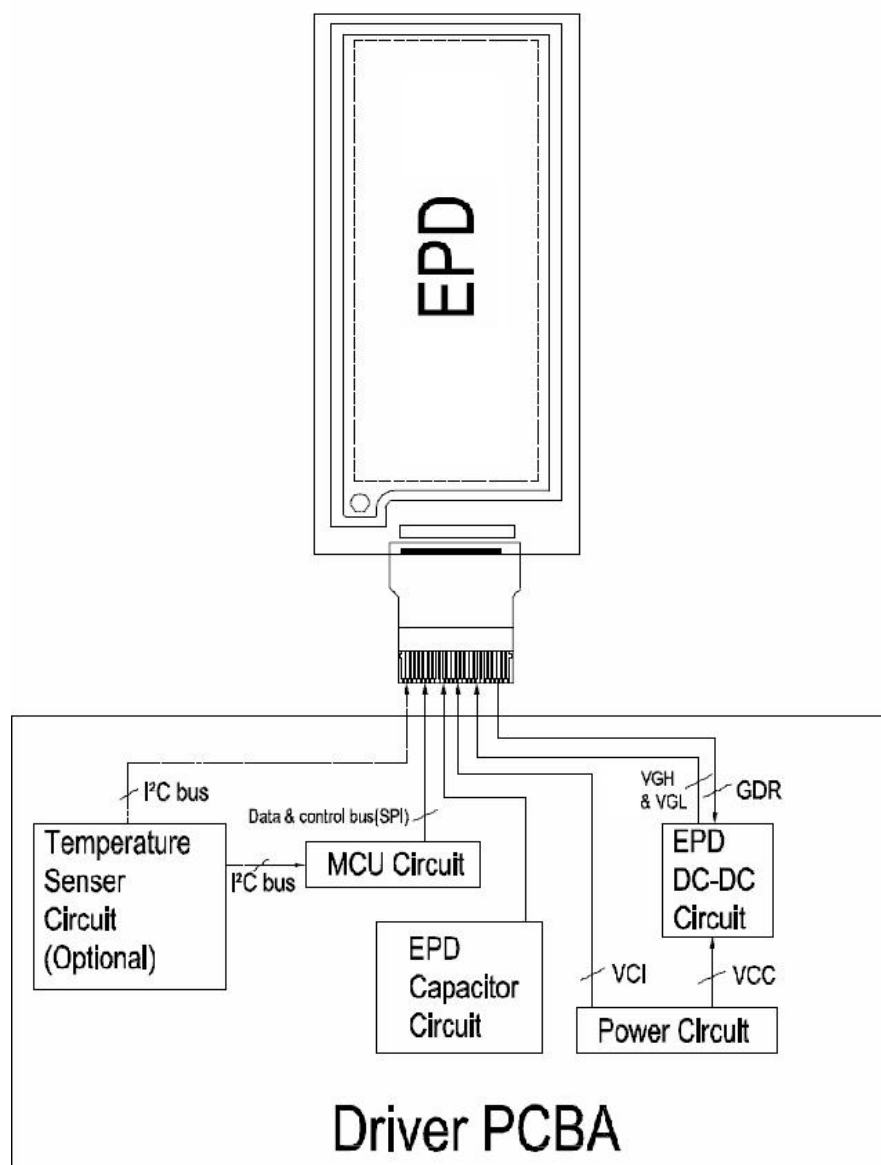
Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

10 Reliability test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	ThermalShock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency:10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence:1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

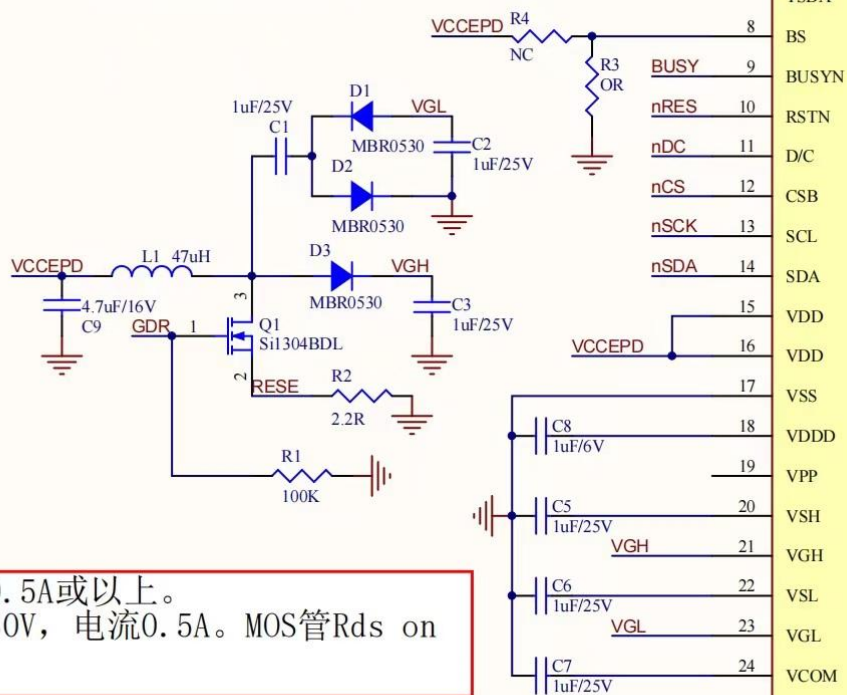
11 Block Diagram



12 Typical Application Circuit with SPI Interface

1. Power Inductor: 47uH, $I > 500\text{mA}$
2. Switch MOS NMOS : $V_{ds} \geq 30\text{V}$, $I_d > 500\text{mA}$, $R_{ds(on)} < 2.1\Omega$, $V_{gs} = 2.5\text{V}$
3. Schottky Diode: $V_r \geq 30\text{V}$, $I_f > 500\text{mA}$

EPD DEMO CIRCUIT



- (1) 功率电感用47uH, 电流0.5A或以上。
 (2) MOS管和二极管具: 耐压30V, 电流0.5A。MOS管 $R_{ds\ on} \leq 2.1\Omega$ @ $V_{gs} = 2.5\text{V}$ 。

EPD_24_INF

13 Point and line standard

1 p u r p o s e

Standardize the inspection standard and sampling proportion of electronic paper modules to ensure that the quality meets the shipment.

2 range of application

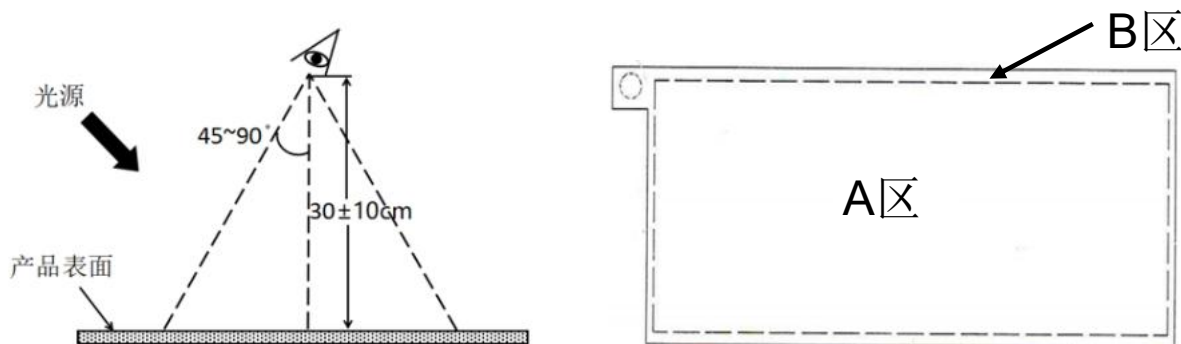
4 check the condition

.1 Temperature requirement: $23\pm 3^{\circ}\text{C}$; Temperature: $60\pm 15\%\text{RH}$

4.2 Check the ambient brightness requirements: the brightness of the appearance check is 700~1000Lux

4.3 Inspection distance: The naked eye is $35\pm 5\text{cm}$ away from the product surface

4.4 Inspection Angle: The eye is perpendicular to the surface of the product, and the front, back, left and right angles are 45. Conduct an inspection



5 definition

5.1 Visual area definition

Area A: display area

Zone B: Edge zone (outside Zone A)

