o Tentative Specification
✓ Preliminary Specification
o Specification Approval

Specification For SID 5.83” BWR EPD

Model Name: JS0583HNV03-TNG-A0

Version:V0.1

SID	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE			

	SIGNATURE	DATE
CUSTOMER APPROVAL		
	Notes:	

Notes :

1、Please contact SID before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	20230214	First release	Preliminary

CONTENTS

1 General Description

SE0583HNV03-A0 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 5.83" active area contains 648×480pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

2 Features

- ◆ 648×480pixels display
- ◆ High contrast
- ◆ High reflectance
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape, portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I2C signal master interface to read external temperature sensor/built-in temperature sensor

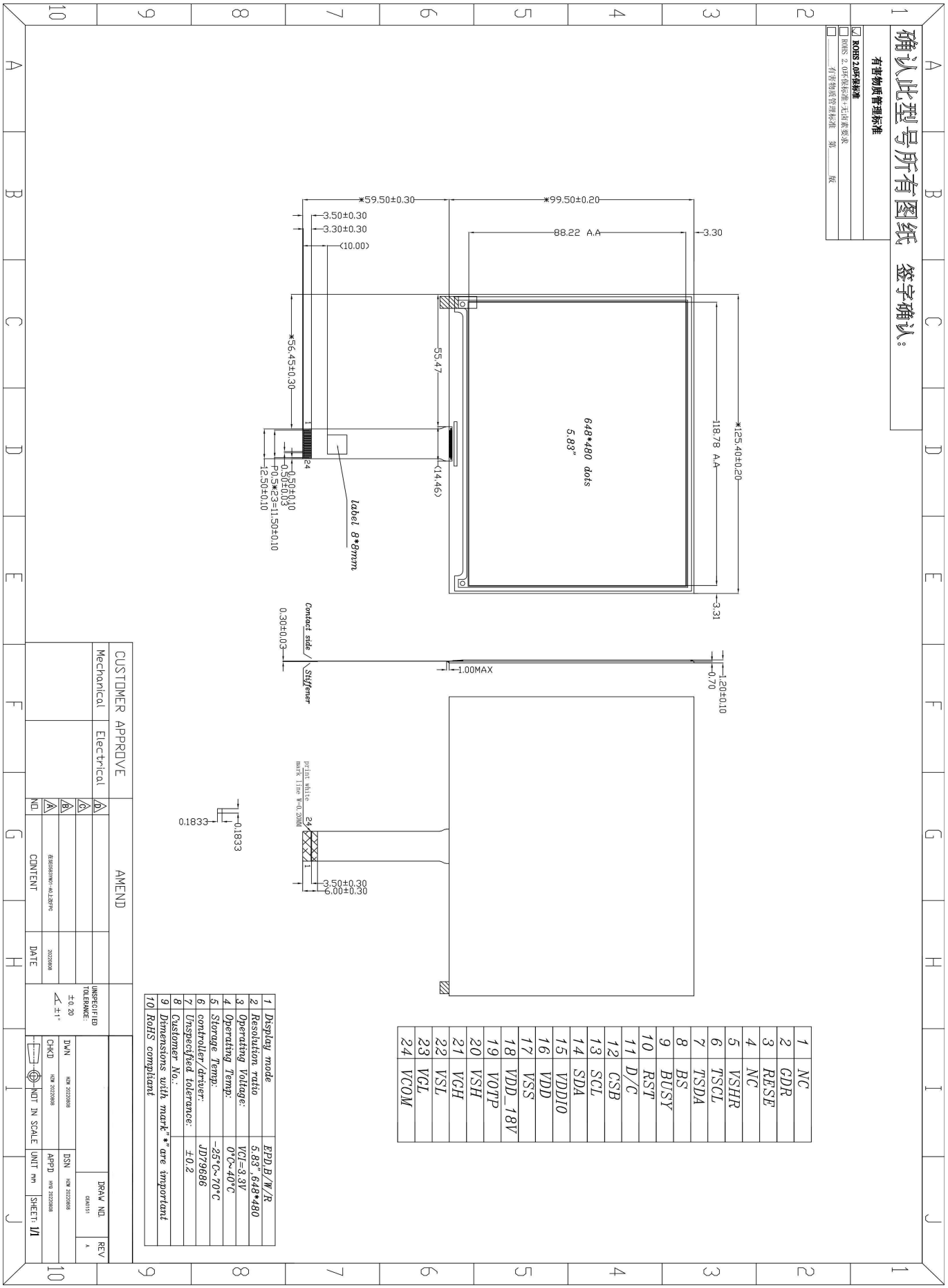
3 Application

Electronic Shelf Label System

4 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	5.83	Inch	
Display Resolution	648(H)×480(V)	Pixel	Dpi:138
Active Area	118.78(H)×88.22(V)	mm	
Pixel Pitch	0.1833×0.1833	mm	
Pixel Configuration	Rectangle		
Outline Dimension	125.4(H)×99.5(V) ×1.20(D)	mm	
Weight	TBD	g	

5 Mechanical Drawing of EPD module



6 Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins e	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSHR	Positive source voltage for Red	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY_N	Busy state output pin	Note 6-4
10	RST_N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	IO voltage supply	
16	VDD	Digital/Analog power.	
17	VSS	Digital ground	
18	VDD_1.8V	1.8V voltage input &output	
19	VOTP	OTP program power (7.5V)	
20	VSH	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.
Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin Low when the driver IC is working such as:

- Outputting display waveform; or

- Communicating with digital temperature sensor

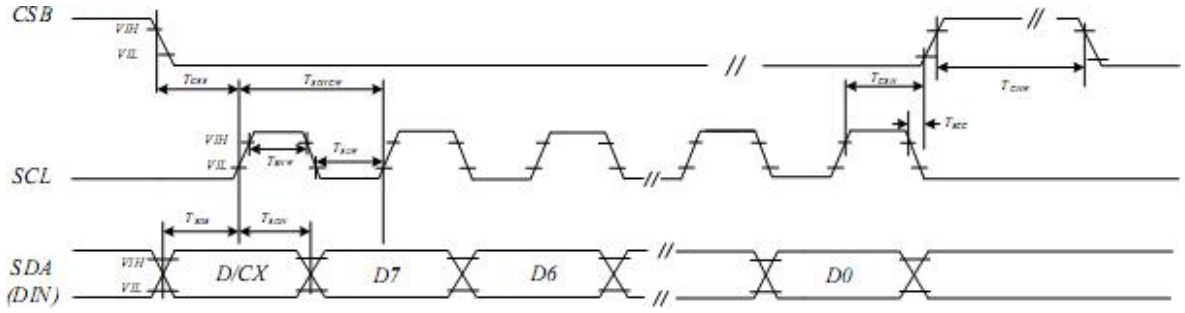
Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7 SPI COMMAND DESCRIPTION

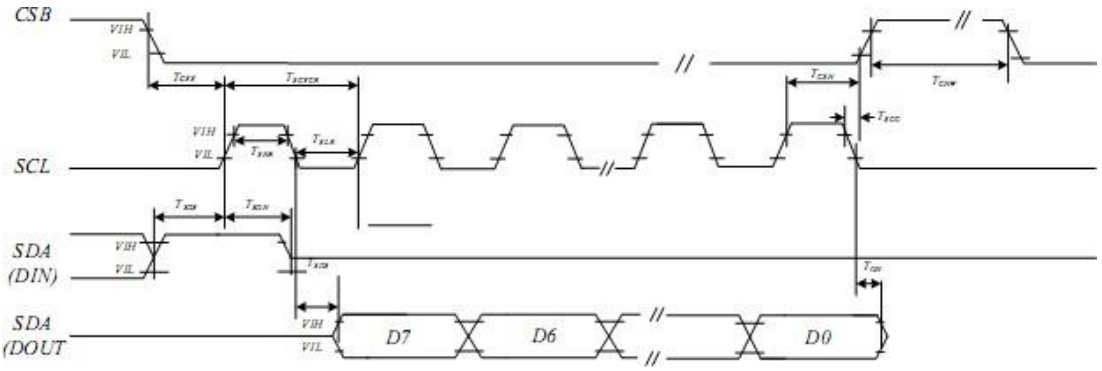
7.1 “3-Wire” Serial Port Interface

E0583A43 use the 3-wire serial port as communication interface for all the function and command setting. 3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79686 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

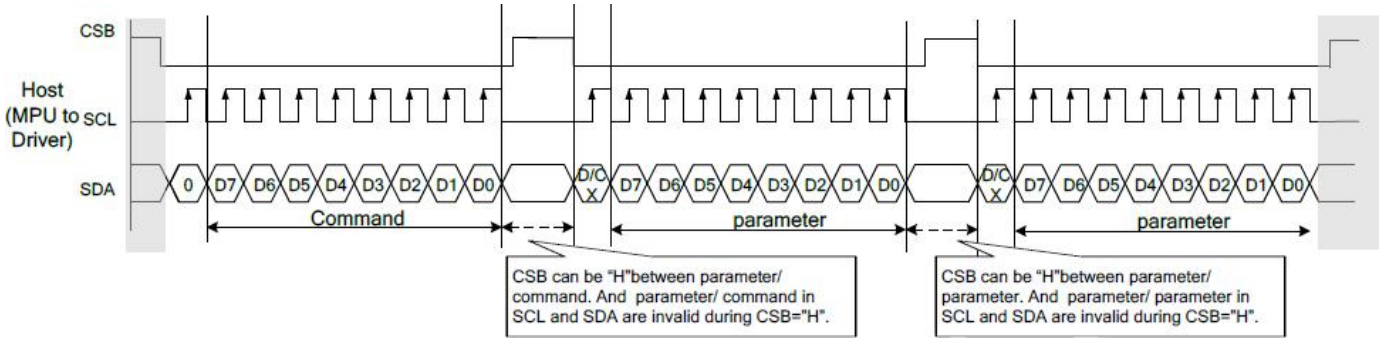
Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”



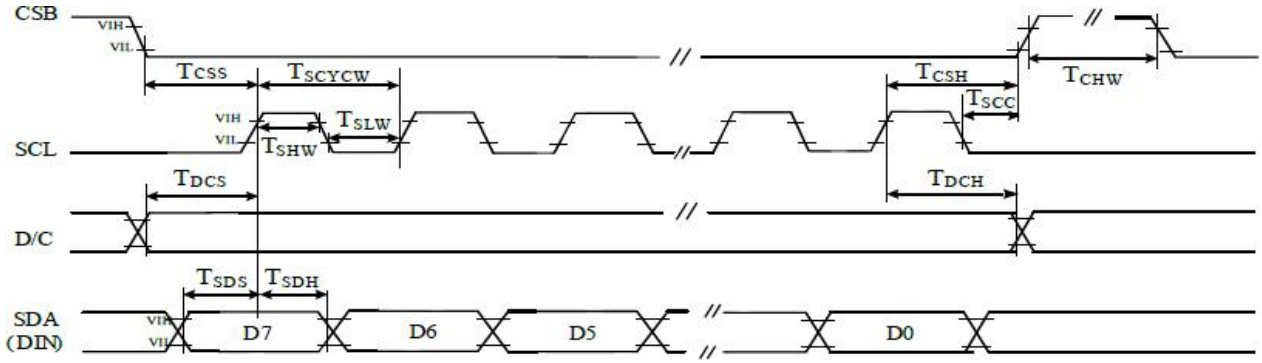
3 pin serial interface characteristics (write mode)



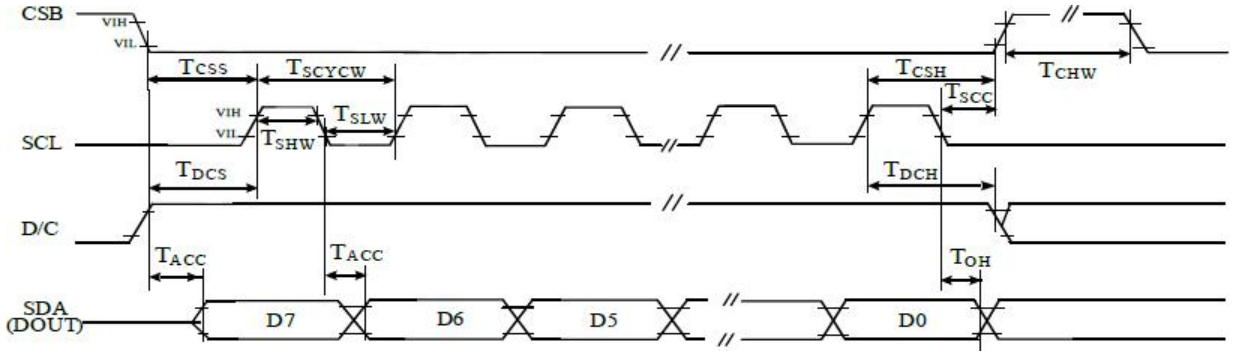
3 pin serial interface characteristics (read mode)



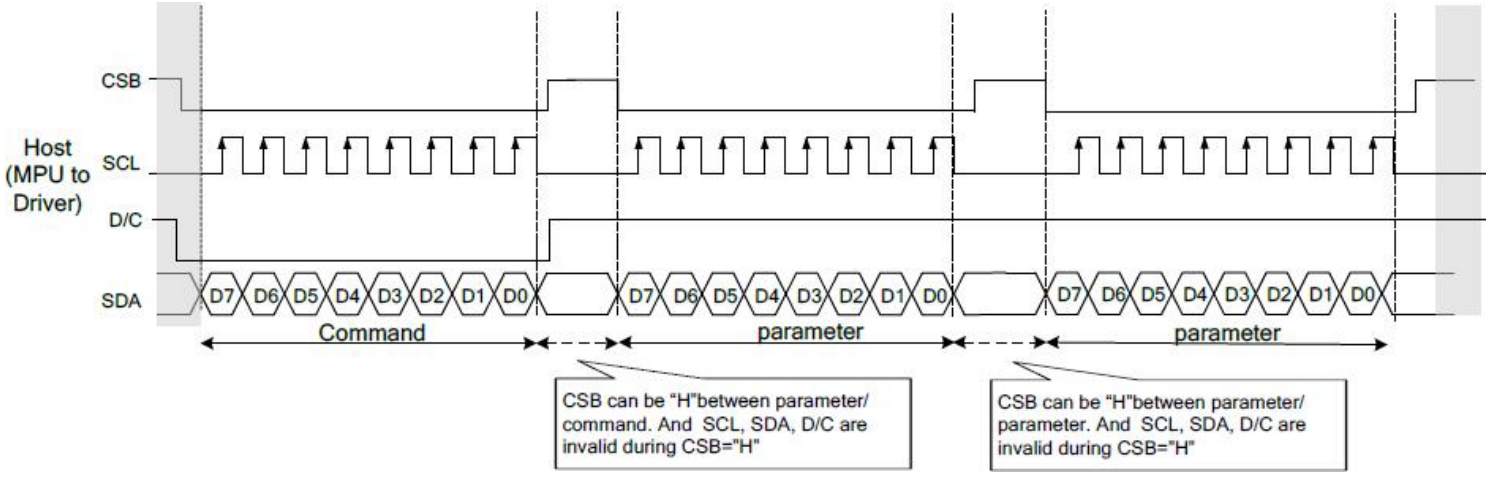
7.2 “4-Wire” Serial Port Interface



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)



8 COMMAND TABLE

8-1Register Table

Following table list all the SPI control registers and bit name definition for EK79686. Refer to the next section for detail register function description.

R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	008H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
		W	1									00H
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3FH
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3bh
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0FH
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF[1]	T_VDS_OFF [0]					00H
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measue (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
		W	1	-		BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission 1 (DTM1)	W	0	0	0	0	1	0	0	0	1	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	-
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R14H	Partial Data Start transmission 1 (PDTM1)	W	0	0	0	0	1	0	1	0	0	14H
		W	1	#	#	#	#	#	#	#	#	00h
R15H	Partial Data Start transmission 2 (PDTM2)	W	0	0	0	0	1	0	1	0	1	15H
		W	1	#	#	#	#	#	#	#	#	00h
R16H	Partial Display Refresh(PF)	W	0	0	0	0	1	0	1	1	0	16H
		W	1	#	#	#	#	#	#	#	#	00h
R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-			M[2:0]		N[2:0]		3Ah	
R40H	TemperatureSensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[8]	D7/TS[7]	D6/TS[9]	D5/TS[8]	D4/TS[10]	D3/TS[9]	--
		R	1	D2	D1	D0	-	-	-	-	-	--
R41H	Temperature Sensor	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

	Calibration (TSE)											
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	-
R60H	TCON setting(TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting (TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00H
		W	1	-	-	-	-	-	-	-	VRES(8)	00H
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00H
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	62H
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	-	-	-	00H
		W	1				gscan				G_start [8]	00H
		W	1	G_start (7)	G_start (6)	G_start (5)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00H
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I2C_ERR	I2C_BUSYN	Data_flag	PON	POF	BUSY_N	-
R81H	Vcom Value (VV)	W	0	1	0	0		0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VCDS[5]	VCDS[4]	VCDS[3]	VCDS[2]	VCDS[1]	VCDS[0]	1Fh
RA0H	Program Mode(PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	1	0	1	A5h
RA1H	Active program(APG)	W	0	1	0	1	0	0	0	0	1	A1H
RA2H	Read OTP Data(ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	-
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h
RE6H	LVD voltage Select	W	0	1	1	1	0	0	1	1	0	E6H
		W	1	-	-	-	-	-	-	LVD_SEL0]	LVD_SEL[0]	11h
RE7H	Panel Break Check	W	0	1	1	1	0	0	1	1	1	E7H
		R	1	-	-	-	-	-	-	-	PSTA	-
RE8H	Power saving	W	0	1	1	1	0	1	0	0	0	E8H
		W	1	-	-	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[2]	SD_W[1]	SD_W[0]	00h
RE9H	AUTO sequence	W	0	1	1	1	0	1	0	0	1	E9H
		W	1	1	0	1	0	0	1	0	1	00h
RECH	Read OTP LUT	W	0	1	1	1	0	1	1	0	0	ECH
		R	1	#	#	#	#	#	#	#	#	-

	backup1											

REDH	OTP LUT backup 2 program	W	0	1	1	1	0	1	1	0	1	EDH
		R	1	#	#	#	#	#	#	#	#	-
REEH	Read OTP LUT backup2	W	0	1	1	1	0	1	1	1	0	EEH
RF0H	Remap LUT	W	0	1	1	1	1	0	0	0	0	F0H
		W	1	-	-	-	bkup_lut_2en	rmp2_table sel[3]	rmp2_table sel[2]	rmp2_table sel[1]	rmp2_table sel[0]	1Fh
		W	1	-	-	-	bkup_lut_1en	rmp1_table sel[3]	rmp1_table sel[2]	rmp1_table sel[1]	rmp1_table sel[0]	1Fh

8-2 Register Description

8-2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh

Description -The command defines as :

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → ⋯→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → ⋯→Sn-1 → Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →⋯→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →⋯→Gn-1 →Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 600x400 11: Display resolution is 640x448

Notes

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.
2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver’s functions will disable. SD output and VCOM will base on previous condition and keep floating.

8-2-2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDS_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default)

2nd Parameter:

Bit	Name	Description
		VGHL_LV Voltage Level. 000: VGH=20 v, VGL=-20v (default) 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v
		VCOM Voltage Level 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. (Default value: 111111b)

Bit	Name	Description
5-0	VSH	Internal VSH power selection. 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v …… 010111: 7.0V 011000: 7.2 V 011001: 7.4 V …. 111010: 14.0V

			111011: 14.2 V 111100: 14.4V 111101: 14.6V 111110: 14.8V 111111: 15.0V
	4th Parameter: Internal VSL power selection for B/W LUT. (Default value: 111111b)		
	Bit	Name	Description
	5-0	VSL	Internal VSL power selection. 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v .... 010111: -7.0V 011000: -7.2 V 011001: -7.4 V .... 111010 :-14.0V 111011: -14.2 V 111100: -14.4 V 111101: -14.6V 111110: -14.8V 111111: -15.0V
	5th Parameter: Internal VSHR power selection for Red LUT. (Default value: 00001111b)		
	Bit	Name	Description
	6-0	VSHR	Internal VSL power selection. 0000000: 2.4 v 0000001: 2.5 v 0000010: 2.6 v 0000011: 2.7 v .... 0101110: 7.0 V 0101111: 7.1 V 0110000: 7.2 V .... 1010001: 10.5V 1010010: 10.6 V 1010011: 10.7 V 1010100: 10.8V 1010101: 10.9V 1010110: 11.0V
	Note: 1.VSH>VSHR		
Restriction			

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. SD output and VCOM will keep floating.
Restriction	

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	Vsh_off[1]	Vsh_off [0]	Vsl_off[1]	vsl_off[0]	vshr_off[1]	vshr_off [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : 1st Parameter:		
	Bit	Name	Description
	1-0	vshr_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
	3-2	vsl_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
	5-4	vsh_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
Restriction			

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as :
	After power on command, driver will power on base on power on sequence. After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.
Restriction	

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as :
	If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	Driving strength of phase A	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase A	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description

	2-0	Driving strength of phase B	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
	5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
	7-6	Soft start period of phase B	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

Description	3rd Parameter:		
	Bit	Name	Description
	2-0	Minimum OFF time setting of GDR in phase C	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
	5-3	Driving strength of phase C	000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
Restriction			

8.2.8 R07H (DSLP): Deep Sleep

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00H
2nd Parameter	W	1									00H
…	W	1									00H
Mth Parameter	W	1	KPixel (n-7)	KPixel(n-6)	KPixel(n-5)	KPixel (n-4)	KPixel(n-3)	KPixel(n - 2)	KPixel (n-1)	KPixel (n)	00H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description -The command defines as :

While finished the data transmitting, user must send this command to driver and read Data_flag information.

1st Parameter:

Bit	Name	Description
7	-	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.

	After “Data Start” (10h) or “Data Stop” (11h) commands and when data_flag=1, BUSY_N signal will become “0” and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = “1”.

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as : While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become “0”.
Restriction	This command only actives when BUSY_N = “1”.

8.2.12R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00H
2nd Parameter	W	1									00H
.....	W	1									00H
Mth Parameter	W	1	KPixel(n-7)	KPixel (n-6)	KPixel (n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel (n)	00H

NOTE: “-” Don’t care, can be set to VDD or GND level

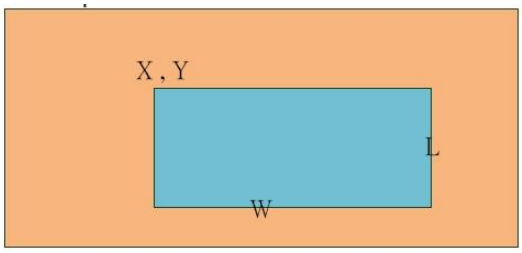
Description	The command define as follows:
	The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes “NEW” data to SRAM. In B/W/Red mode, this command writes “RED” data to SRAM.
Restriction	

8.2.13 R14H (PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h

4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel 5	KPixel 6	KPixel 7	KPixel 8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel (n-3)	KPixel (n-2)	KPixel (n-1)	KPixel (n)	00h

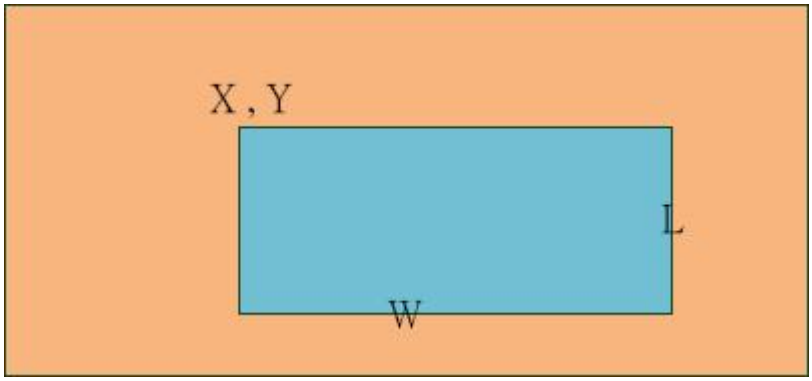
NOTE: “-” Don’t care, can be set to VDD or GND level

Description	The command define as follows:
	The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes “OLD” data to SRAM. In B/W/Red mode, this command writes “B/W” data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.14 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

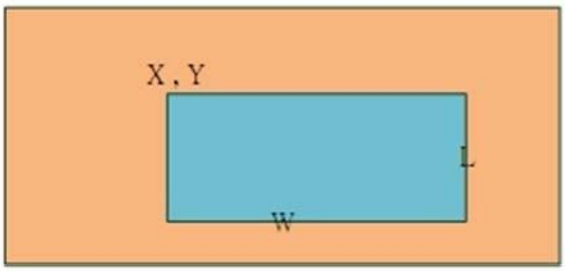
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.15 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	DFV_EN						X[9]	X[8]	00h
2nd Parameter			X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter	W	1							Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	00h
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	
8th Parameter			L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows:
	While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

8.2.16 R30H (OSC): OSC control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: “-” Don’t care, can be set to VDD or GND level

Description

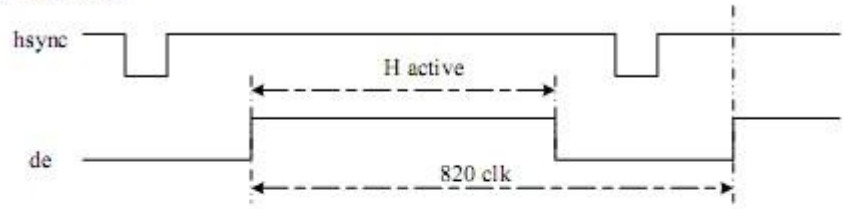
-The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

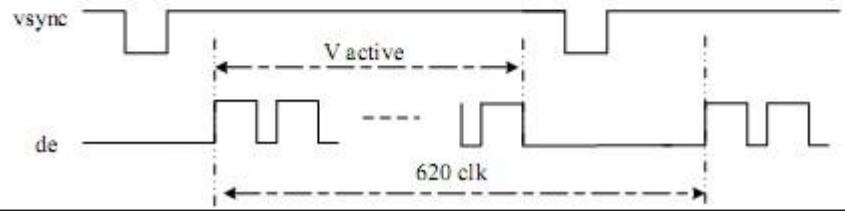
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

8.2.17 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS [7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	-

NOTE: “-” Don’t care, can be set to VDD or GND level

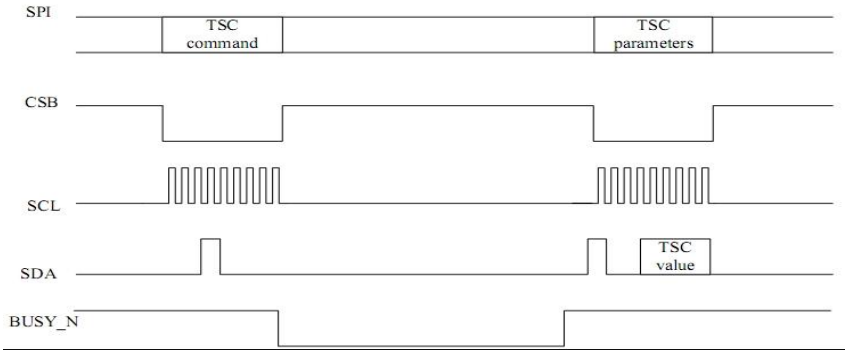
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (° C)	TS[7:0]/D[10:3]	T (° C)	TS[7:0]/D[10:3]	T (° C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction: This command only actives after R04H(PON) or R05H(PMES)

8.2.18 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function.	
	Bit	temperature
	2-0	mean temperature offset value 000:0℃ 001:1℃ 010:2℃ …. 111:7℃
	3	Positive and negative value 0:” +” 1: ” - “
	7	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.
	For example: 1100: - 4 degree c 0111: + 7 degree c	
Restriction	This command only actives after R04H(PON) or R05H(PMES)	

8.2.19 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command writes the temperature. 1st Parameter:	
	Bit	temperature
	2-0	Pointer setting
	5-3	User-defined address bits (A2, A1, A0)
	7-6	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

	2nd Parameter:	
	Bit	temperature
	7-0	MSByte of write-data to external temperature sensor
	3nd Parameter:	
	Bit	temperature
	7-0	LSByte of write-data to external temperature sensor
Restriction	This command only actives after R04H(PON) or R05H(PMES)	

8.2.20 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	1	43H
1st Parameter	R	1	RMSB[7]	RMSB [6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB [1]	RMSB [0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command reads the temperature sensed by the temperature sensor. 1st Parameter:	
	Bit	temperature
	7-0	MSByte of read-data from external temperature sensor
	2nd Parameter:	
	Bit	temperature
	7-0	LSByte of write-data from external temperature sensor
Restriction	This command only actives after R04H(PON) or R05H(PMES)	

8.2.21 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery’s condition. When LPD=”1”, system input power is normal. When LPD=”0”, system input power is lower (VDD<2.5v, which could be select in RE6H (LVSEL)). 1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status

Restriction	

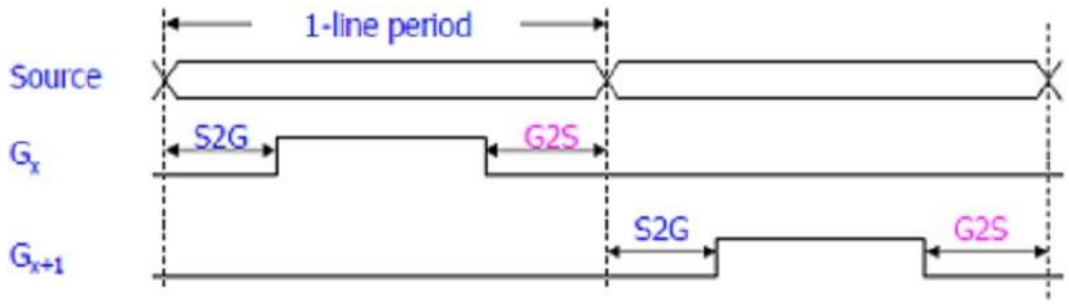
8.2.22 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	- The command define Non-overlap period of gate and source as below: 1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 4 clock(default) 0001: 8 clock 0010: 12 clock 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

	Period=660n s 
Restriction	

8.2.23 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1							HRES (9)	HRES (8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
3rd Parameter	W	1							VRES (9)	VRES (8)	00h
4th Parameter	W	1	VRES(7	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127)
Restriction	

8.2.24 R62H (TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1							S_Start (9)	S_Start (8)	00h
2nd Parameter	W	1	S_Start (7)	S_Start (6)	S_Start (5)	S_Start (4)	S_Start (3)	-	-	-	00h
3rd Parameter	W	1				gscan			G_Start (9)	G_Start (8)	00h
4th Parameter	W	1	G_Start (7)	G_Start (6)	G_Start (5)	G_Start (4)	G_Start (3)	G_Start (2)	G_Start (1)	G_Start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

8.2.25 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The LUT_REV is read from OTP address = 0x001.& 0x002
Restriction	- This command only actives when BUSY_N = "1".

8.2.26 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1			I2C_ERR	II2C_BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
5	I2C master error status

	4	I2C master busy status (low active)
	3	Driver has already received one frame data
	2	PON 0: Not in PON mode 1: In PON mode
	1	POF 0: Not in POF mode(default) 1: In POF mode
	0	Driver busy status(low active)
Restriction	User can send this command in any time. It doesn’t have restriction of BUSY_N.	

8.2.27 R81H (VV): Vcom Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: This command could get the Vcom value 1st Parameter:	
	Bit	Function
	5-0	Vcom value 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V
Restriction	This command only actives when BUSY_N = “1”.	

8.2.28 R82H (VDCS): Vcom_DC Setting register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1st Parameter:

Bit	Function
5-0	VCOM value 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V

Restriction	This command only actives when BUSY_N = “1”.

8.2.29 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = “1”.

8.2.30 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

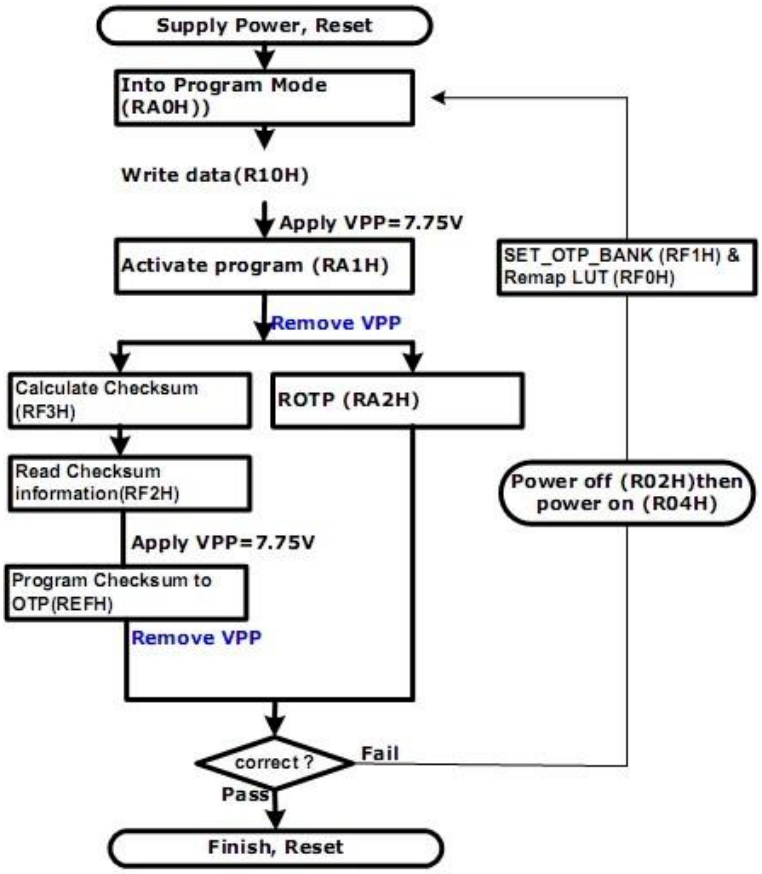
NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.31 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~ (m-1)th Parameter	R	1	…								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.  The sequence of programming OTP
Restriction	This command only actives when BUSY_N = “1”.

8.2.32 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	This command is used for cascade.	
	1st Parameter:	
	Bit	
	0	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
	1	Let the value of slave’s temperature is same as the master’s. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
Restriction	This command only actives when BUSY_N = “1”.	

8.2.33 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET [6]	TS_SET [5]	TS_SET [4]	TS_SET [3]	TS_SET[2]	TS_SET [1]	TS_SET [0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows:
	This command is used to fix the temperature value of master and salve
Restriction	

8.2.34 RE6H (LVSEL): LVD voltage Select

RE6H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	0	E6H
1st Parameter	W	1							LVD_SEL[1]	LVD_SEL[0]	11h

Description	LVD_SEL[1:0]: Low power Voltage selection	
	LVD_SEL[1:0]	LVD value
	00	< 2.2 V
	01	< 2.3 V
	10	< 2.4 V
	11	< 2.5 V
Restriction		

8.2.35RE7H (PBC): Panel Break Check

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1								PSTA	-

Description`	This command is used to enable panel check, and to disable after reading result. 1st Parameter:

Bit	PSTA
0	Panel check fail (panel broken).
1	Panel check pass

Restriction	

8.2.36 RE8H (PWS): Power Saving

RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Power Saving	W	0	1	1	1	0	0	1	1	1	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00H

Description	This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter: Vcom_W[3:0]: VCOM power saving width (unit = line period)
Restriction	

8.2.37 RE9H (AUTO): AUTO Sequence

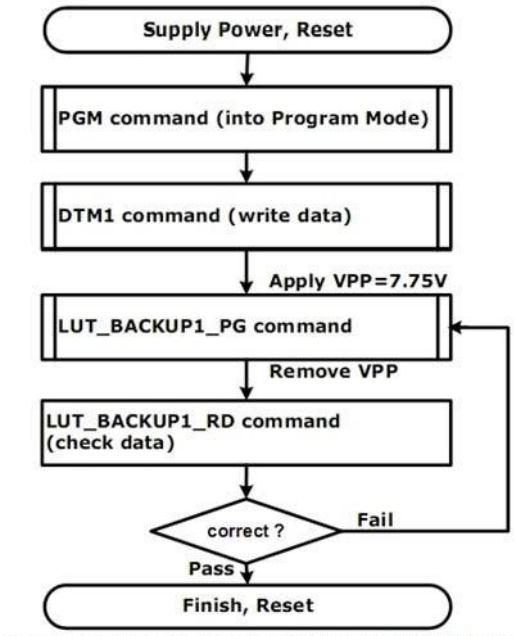
RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO Sequence	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00H

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

8.2.38RECH (LUT_BACKUP1_RD): Read OTP LUT backup1

RECH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP1_RD	W	0	1	1	1	0	1	1	0	0	ECH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xA00/0x1600 in the OTP								
3rd Parameter	R	1	The data of address 0xA01/0x1601 in the OTP								
4th Parameter	R	1	The data of address 0xA02/0x1602 in the OTP								
5th Parameter	R	1	The data of address 0xA03/0x1603 in the OTP								
6th~ 256th Parameter	R	1	….								
257th Parameter	R	1	The data of address 0xAFF/0x16FF in the OTP								

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.  The sequence of programming OTP LUT backup1
Restriction	This command only actives when BUSY_N = “1”.

8.2.39 REDH (LUT_BACKUP2_PG): OTP LUT backup2 program

REDH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_PG	W	0	1	1	1	0	1	1	0	1	EDH

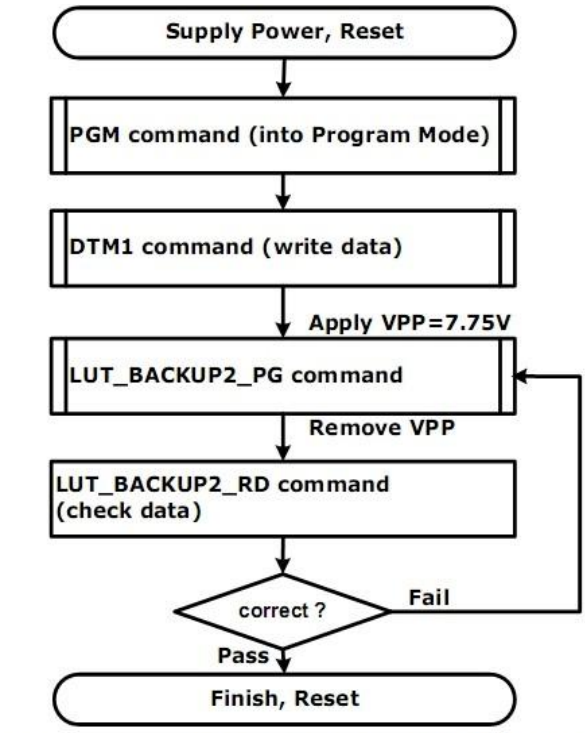
NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.40 REEH (LUT_BACKUP2_RD): Read OTP LUT backup2

REEH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_RD	W	0	1	1	1	0	1	1	1	0	EEH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xB00/0x1700 in the OTP								
3rd Parameter	R	1	The data of address 0xB01/0x1701 in the OTP								
4th Parameter	R	1	The data of address 0xB02/0x1702 in the OTP								
5th Parameter	R	1	The data of address 0xB03/0x1703 in the OTP								
6th~ 256th Parameter	R	1	….								
257th Parameter	R	1	The data of address 0xBFF/0x17FF in the OTP								

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.  The sequence of programming OTP LUT backup2
Restriction	This command only actives when BUSY_N = “1”.

8.2.41 RF0H (RM_LUT_CMD): Remap LUT command

RF0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RM_LUT_CMD	W	0	1	1	1	1	0	0	0	0	F0H
1st Parameter	W	1	-	-	-	r10_lut_en	mp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
2nd Parameter	W	1	-	-	-	tr9_lut_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh

NOTE: “-” Don’t care, can be set to VDD or GND level

Description

The command is used for indicating backup OTP blocks to remap for LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h	TR0 WF	D00h	TR0 WF
200h	TR1 WF	E00h	TR1 WF
300h	TR2 WF	F00h	TR2 WF
400h	TR3 WF	1000h	TR3 WF
500h	TR4 WF	1100h	TR4 WF
600h	TR5 WF	1200h	TR5 WF
700h	TR6 WF	1300h	TR6 WF
800h	TR7 WF	1400h	TR7 WF
900h	TR8 WF	1500h	TR8 WF
A00h	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
B00h	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

1st Parameter:
tr10_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as “TR10 WF”
0	OTP Address B00h~BFFh is used as “Backup 2”, And you can replace one of TR0 ~TR9.

rmp2_tab_sel [3:0] :

Only be functional when tr10_lut_en is set “0”, target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010	TR9
1011~1111	None

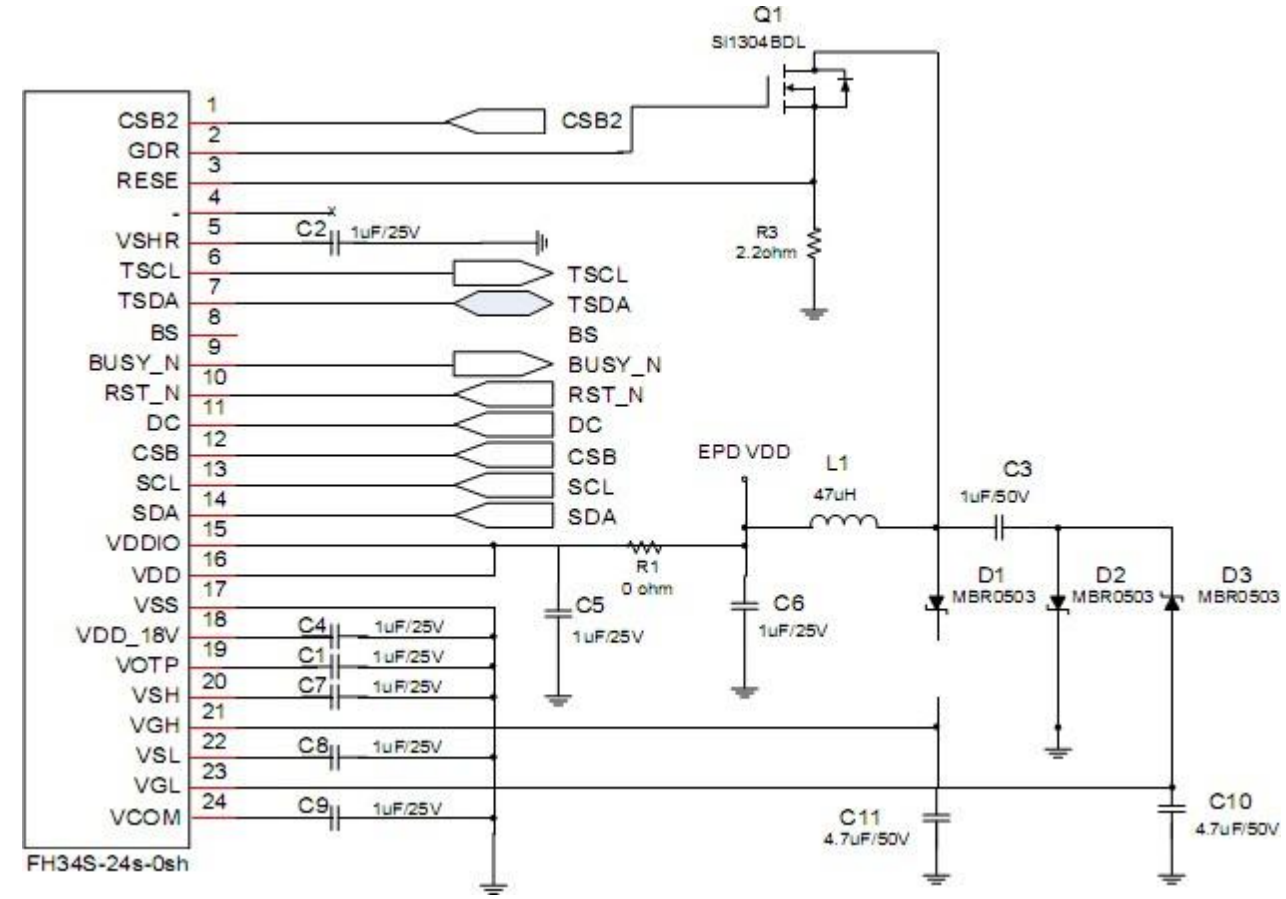
2nd Parameter tr9_lut_en :

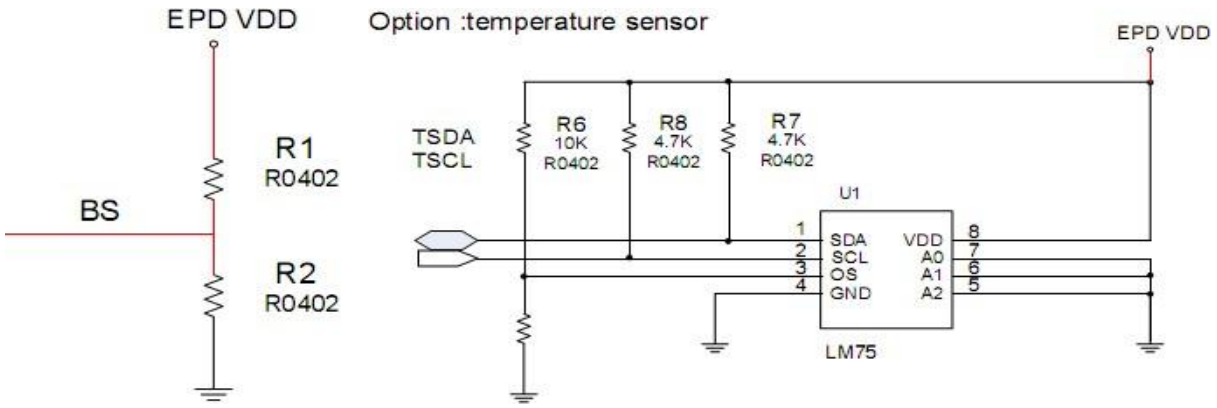
Value	Function

<table>
<tr><td></td><td>
<table>
<tr><td>1</td><td>OTP Address B00h~BFFh is used as “TR9</td></tr>
<tr><td>0</td><td>OTP Address B00h~BFFh is used as “Backup 1”, And you can replace one of TR0</td></tr>
</table>
rmp1_tab_sel[3:0]

Only be functional when tr9_lut_en is set “0”, target LUTs to be replaced is
<table>
<tr><td>Value</td><td>Target</td></tr>
<tr><td>0001</td><td>TR0</td></tr>
<tr><td>0010</td><td>TR1</td></tr>
<tr><td>0011</td><td>TR2</td></tr>
<tr><td>0100</td><td>TR3</td></tr>
<tr><td>0101</td><td>TR4</td></tr>
<tr><td>0110</td><td>TR5</td></tr>
<tr><td>0111</td><td>TR6</td></tr>
<tr><td>1000</td><td>TR7</td></tr>
<tr><td>1001</td><td>TR8</td></tr>
<tr><td>1010~1111</td><td>None</td></tr>
</table>
Notice :
If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload “backup 1” block to replace target LUT.
</td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

9 Reference Circuit





	R1	R2
3- wire SPI (CS#, SDA, SCL)	10K	NC
4-wire SPI (D/C#, CS#, SDA, SCL)	NC	10K

Note:

Part name	Value / Type	Requirement / Reference part
C1, C2, C4-C9	1uF	0603, X5R/X7R, Voltage Rating:25V
C3	1uF	0603, X5R/X7R, Voltage Rating:50V
C10,C11	4.7uF	0805, X5R/X7R, Voltage Rating:50V
R2	2.2Ω	0603; 1% variation
D1-D3	Diode	MBR0530 1. Reverse DC voltage ≧ 30V 2. Forward current ≧ 500mA 3. Forward voltage ≦ 430mV
Q1	NMOS	Si1308EDL / Si1304BDL 1. Drain-source break volatage ≧ 30V 2. Gate-source threshold voltage ≦ 1.5V 3. Drain-source on-state resistance < 400mΩ
L1	47uH	CDRH2D18 / LDNP-470NC 1. Maximum DC current~420Ma 2. Maximum DC resistance~650mΩ

10 ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.3 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 40	°C	45 to70	%	Note 10-1
Tttg	Transportation temperature range	-25 to 60	°C	-	-	Note10-2
Tstg	Storage condition	0 to 40	°C	45 to70	%	
-	After opening the package	0 to 40	°C	45 to70	%	

Note 10-1：We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note10-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 40℃ ~60℃. Note 10-3：When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months. We suggest that the full black and full white picture could be added to clear the screen after the module is refreshed for a long time, the display effect would be better.

11 DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃.

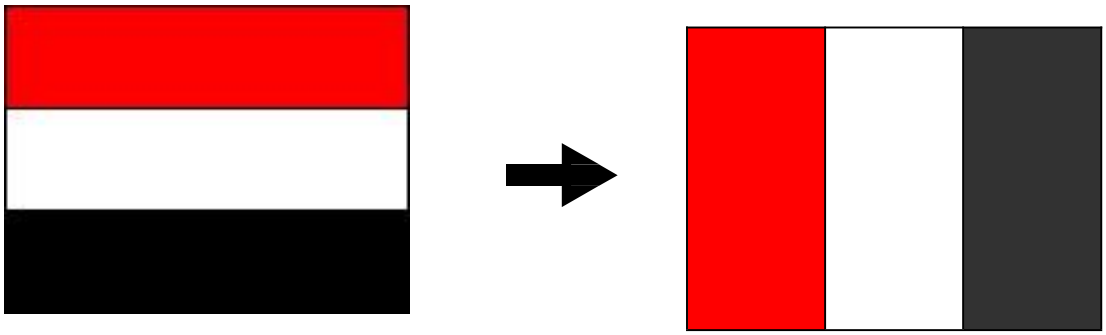
Table 11-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	
VCI	Logic supply voltage	-	VCI	2.5	3.3	3.6	V
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.7VDDIO	-	VIO	V
VIL	Low level input voltage	-		GND	-	0.3VDDIO	V
VOH	High level output voltage	IOH = 400uA	BUSY,	VIO-0.4	-	-	V
VOL	Low level output voltage	IOL = -400uA		-	-	GND+0.4	V
Iupdate	Module operating current	-	-	-	6.5	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	-	3	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption



12 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.5V to 3.6V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CSB has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CSB has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

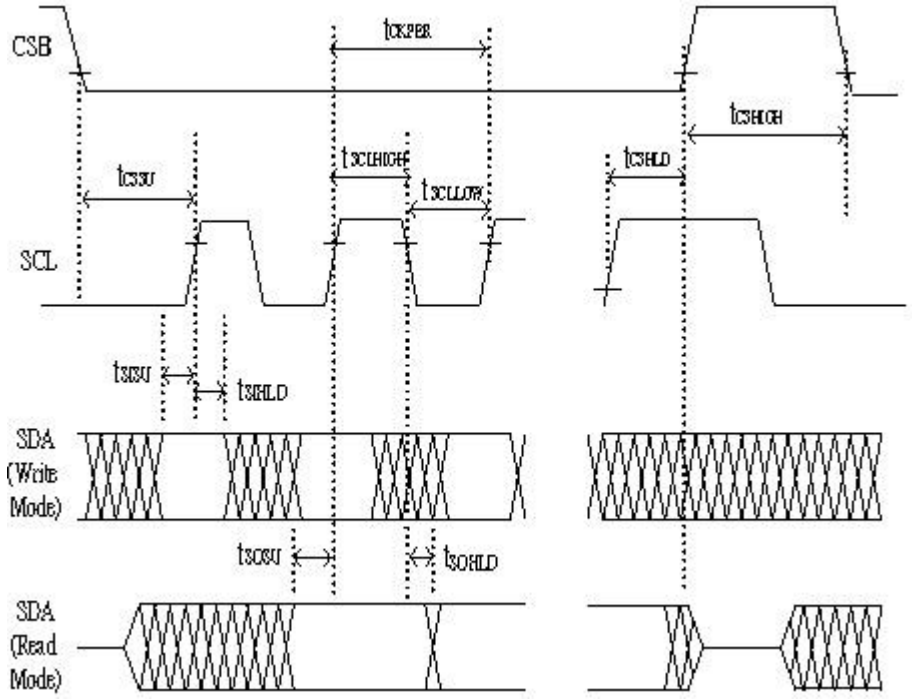


Figure 14-1: Serial peripheral interface characteristics

13 Power ON/OFF Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power ON Sequence

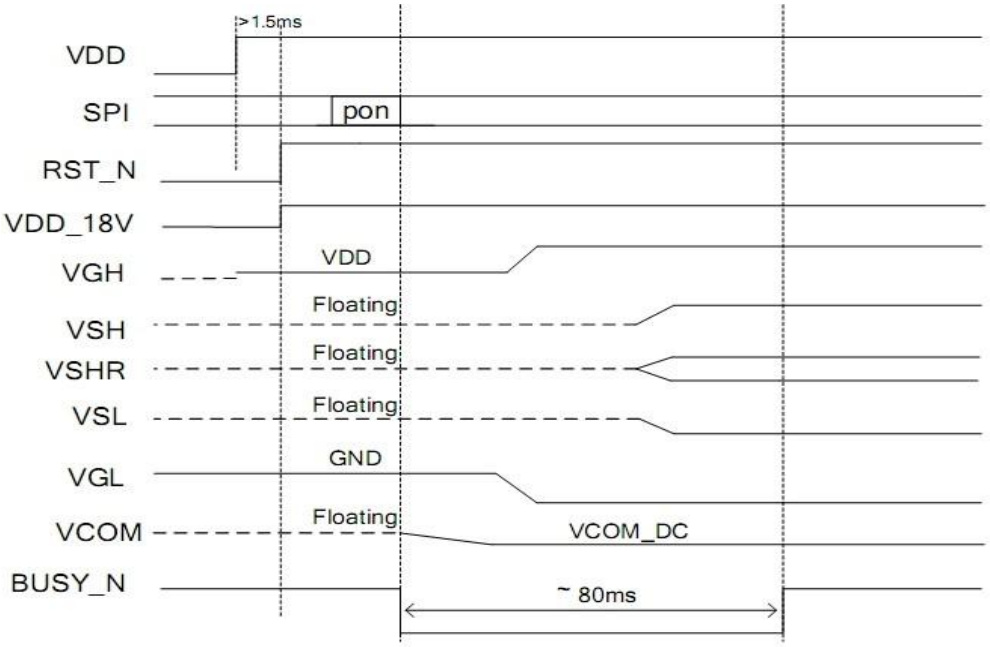


Figure 1: Power on sequence

Power OFF Sequence

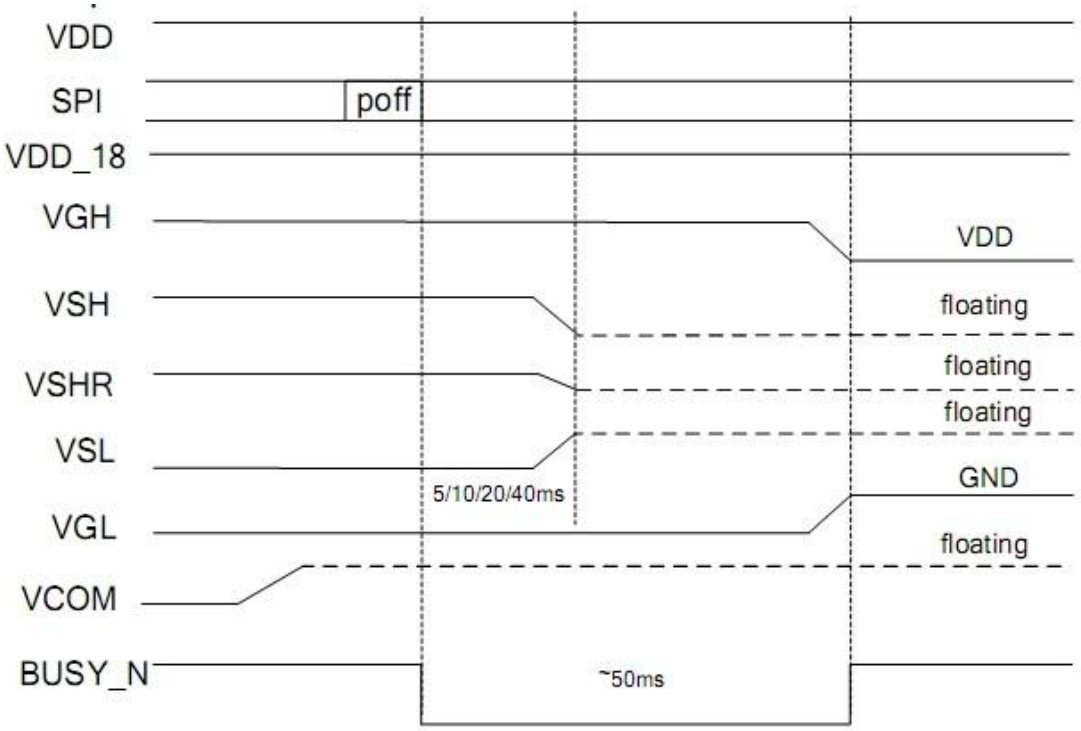


Figure 2: Power off sequence

DSLP sequence

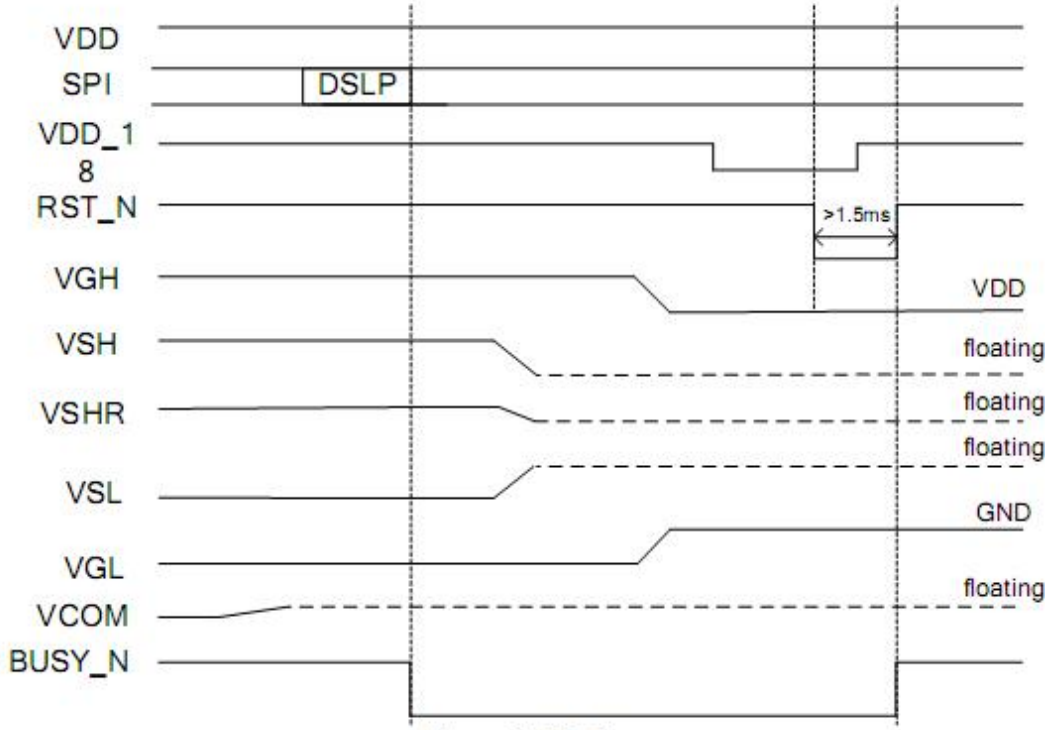


Figure 3: DSLP sequence

14 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	140	-	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

mAs=update average current×update time

15 Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless
otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
KS	Black State L* value		-	13	14		Note 15-1
	Black State a* value		-	3	5		Note 15-1
WS	White State L* value		63	65	-		Note 15-1
RS	Red State L* value	Red	25	28	-		Note 15-1
	Red State a* value	Red	36	40	-		Note 15-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

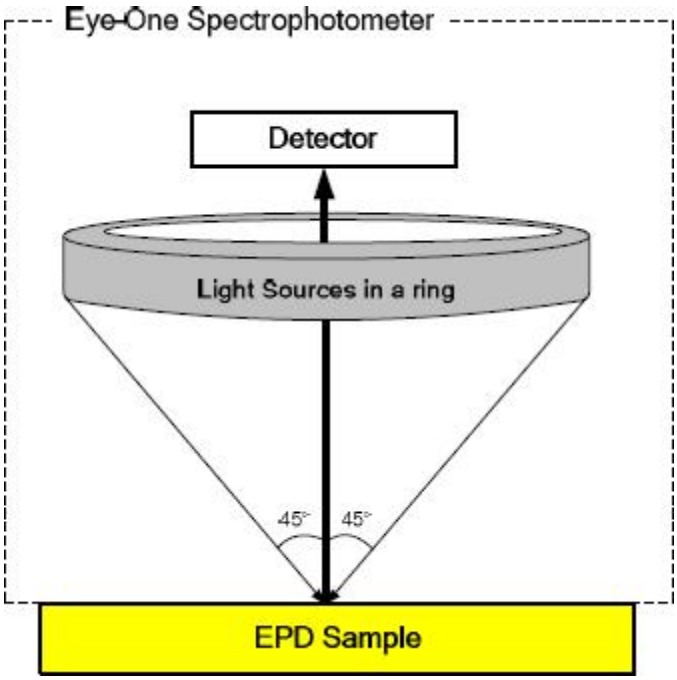
WS : White state, KS : Black state, RS: Red state

Note 15-1 : Luminance meter : i - One Pro Spectrophotometer

15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd)：

CR = Rl/Rd

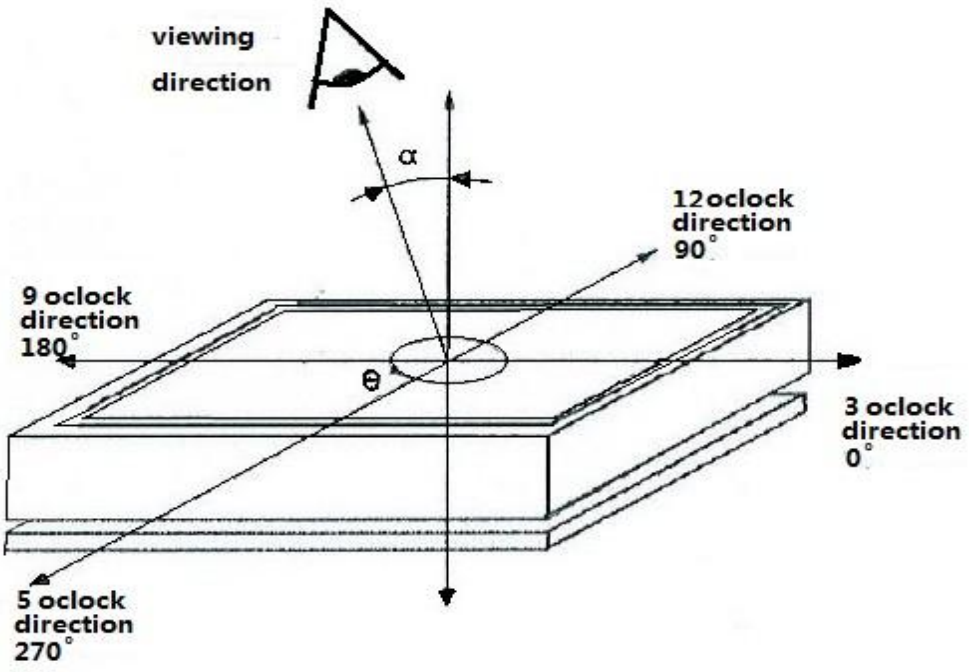


15.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



16 HANDLING,SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

17 Reliability test

17.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=50℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=50℃,RH=80%RH,For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min),50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed shipment for
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed shipment for
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

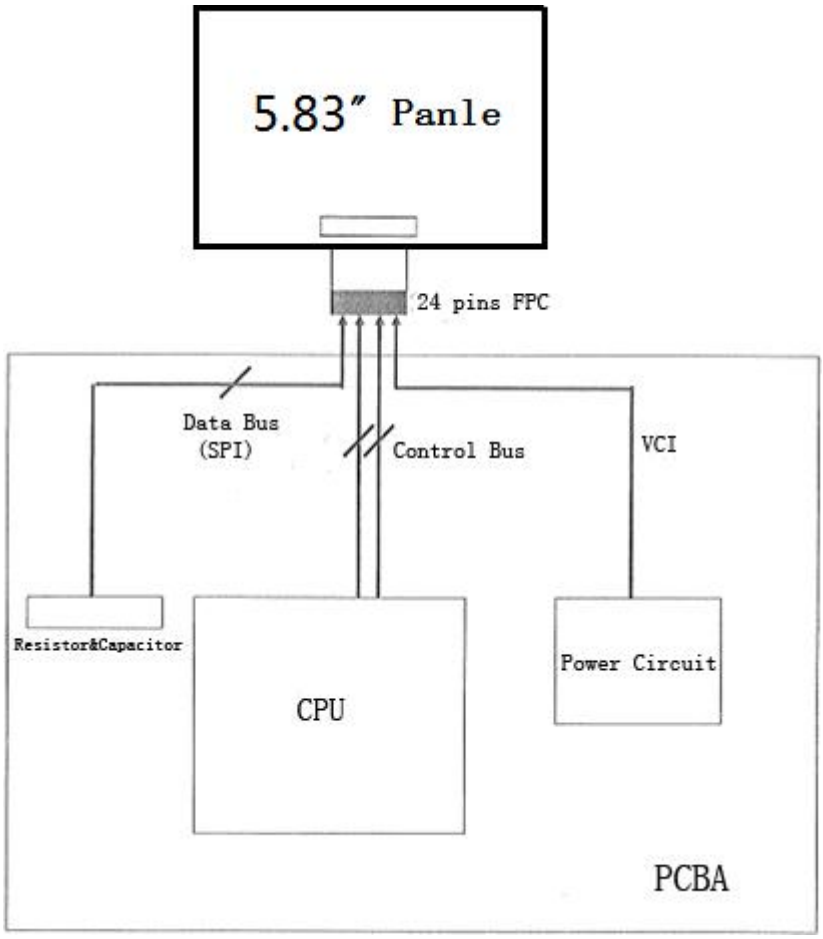
Note1：Stay white pattern for storage and non-operation test. Note2：Operation is black/white/red pattern , hold time is 150S.

Note3：The function ,appearance, opticals should meet the requirements of the test before and after the test. Note4：Keep testing after 2 hours placing at 20℃-25℃.

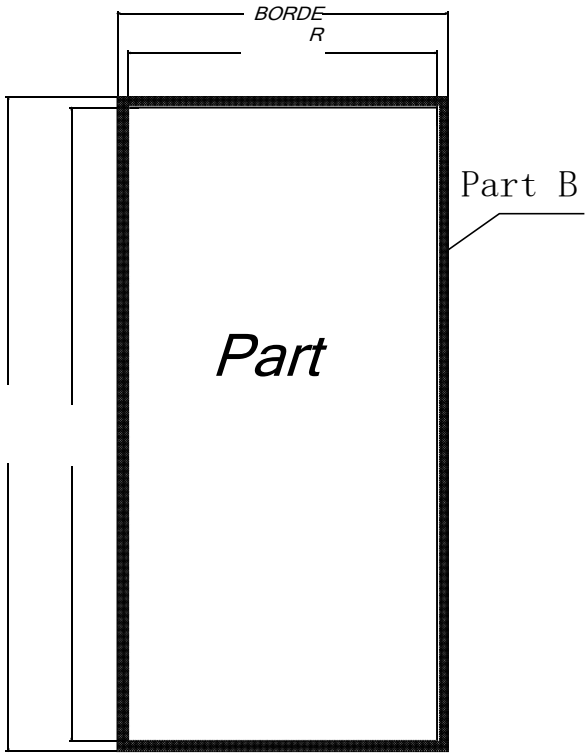
17.2 Product life time

The EPD Module is designed for a 5-year life-time with 25 ℃/60%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

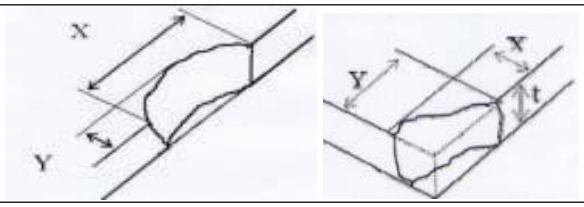
18 Block Diagram

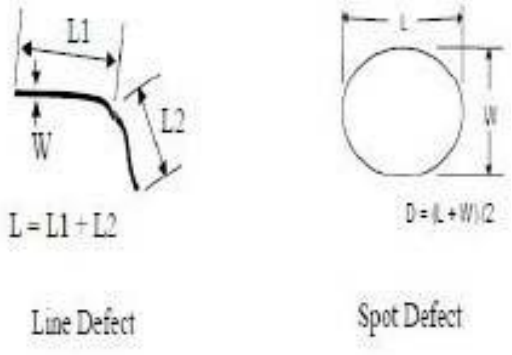


19 PartA/PartB specification



20 Point and line standard

<table>
<tr><th colspan="8">Shipment Inspection Standard</th></tr>
<tr><td colspan="8">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>125.4(H)×99.5(V)
×1.10(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td colspan="2">Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td colspan="2">Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5%RH</td><td>800～1300Lux</td><td>300 ㎜</td><td>35Sec</td><td colspan="2"></td></tr>
<tr><td>Defect type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td colspan="2">Part-B</td></tr>
<tr><td rowspan="4">Spot</td><td rowspan="4">Electric Display</td><td colspan="2">D≤0.2 ㎜</td><td colspan="2">Ignore</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">0.2 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">0.4 ㎜＜D≤0.6 ㎜</td><td colspan="2">N≤1</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">D＞0.6 ㎜</td><td colspan="2">Not Allow</td><td colspan="2">Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td colspan="2">Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td colspan="2">Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">L≤2 ㎜,W≤0.1 ㎜</td><td colspan="2">Ignore</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">2.0mm＜L≤9.0mm,0.1＜W≤
0.2mm,</td><td colspan="2">N≤2</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">L＞9.0 ㎜,W＞0.2 ㎜</td><td colspan="2">Not Allow</td><td colspan="2">Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.4mm</td><td colspan="2">Ignore</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">0.4mm≤D≤0.6mm</td><td colspan="2">N≤4</td><td colspan="2">Ignore</td></tr>
<tr><td colspan="2">D＞0.6 mm</td><td colspan="2">Not Allow</td><td colspan="2">Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="6">Do not affect the electrode circuit((Corner chipping)
X≤8mm,Y≤1mm, Do not affect the electrode circuit, Ignore</td></tr>
<tr><td colspan="6"> 
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="7">1. Appearance defect should not cause electrical defects；</td></tr>
<tr><td colspan="7">2. Appearance defects should not cause dimensional accuracy problems</td></tr>
<tr><td colspan="7">L=long W=wide D=point size N=Defects NO</td></tr>
</table>



Line Defect Spot Defect

L=long W=wide D=point size