



Specification For SID 7.50” BW EPD

Model Name JS0750NW20-MNG-A0

Version: V0.2

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CONTENTS

| | |
|--|-----------|
| 1 General Description | 4 |
| 2 Features | 4 |
| 3 Application | 4 |
| 4 Mechanical Specification | 4 |
| 4.1 Dimension | 4 |
| 4.2 Mechanical Drawing of EPD Module | 5 |
| 5 Input/output Pin Assignment | 6 |
| 6 Electrical Characteristics | 7 |
| 6.1 Absolute Maximum Rating | 7 |
| 6.2 Panel DC Characteristics | 7 |
| 6.3 Panel DC Characteristics(Driver IC Internal Regulators) | 8 |
| 6.4 Panel AC Characteristics | 9 |
| 7 Optical Specification | 13 |
| 8 Handling, Safety, and Environment Requirements | 14 |
| 9 Reliability Test | 15 |
| 10 Block Diagram | 16 |
| 11 Typical Application Circuit with SPI Interface | 17 |

N1 General Description

JS0750NW20-MNG-A0 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 7.5” active area contains 800x480 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 800×480pixels display
- ◆ White reflectance above 30%
- ◆ Contrast ratio above 8:1
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I2C signal master interface to read external temperature sensor

3 Application

Electronic Shelf Label System

4 Mechanical Specification

4.1 Dimension

| Parameter | Specifications | Unit |
|---------------------|-------------------------------|-------|
| Screen Size | 7.5 | Inch |
| Display Resolution | 800(H)×480(V) | Pixel |
| Active Area | 163.20(H) × 97.92 (V) | mm |
| Pixel Pitch | 204(H) × 204(V) | um |
| Pixel Configuration | Rectangle | |
| Outline Dimension | 170.2 (H) × 111.2(V) ×1.07(D) | mm |

5 Input/output Pin Assignment

| No. | Name | I/O | Description | Remark |
|-----|-------|-----|---|----------|
| 1 | NC | | Do not connect with other NC pins | |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | | Do not connect with other NC pins | |
| 5 | VDHR | C | Positive Source driving voltage 1 | |
| 6 | TSCL | O | I2C Interface to digital temperature sensor Clock pin | |
| 7 | TSDA | I/O | I2C Interface to digital temperature sensor Data pin | |
| 8 | BS | I | Bus Interface selection pin | Note 5-4 |
| 9 | BUSYN | O | Busy state output pin | Note 5-3 |
| 10 | RSTN | I | Reset signal input. Active Low. | |
| 11 | D/C | I | Data /Command control pin | Note 5-2 |
| 12 | CSB | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I | Serial Data pin (SPI) | |
| 15 | VDD | P | Power Supply for interface logic pins | |
| 16 | VDD | P | Power Supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDDD | C | Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances | |
| 19 | VPP | P | Power Supply for OTP Programming | |
| 20 | VSH | C | Positive Source driving voltage 2 | |
| 21 | VGH | C | Positive Gate driving voltage | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Negative Gate driving voltage | |
| 24 | VCOM | C | VCOM driving voltage | |

I = Input Pin, O = Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

| BS State | MCU Interface |
|----------|--|
| L | 4-lines serial peripheral interface(SPI) |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

6 Electrical Characteristics

6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|----------------------|--------|------------------|------|
| Logic supply voltage | Vdd | -0.3 to +6.0 | V |
| Logic Input voltage | VIN | -0.3 to Vdd +0.3 | V |

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operations should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

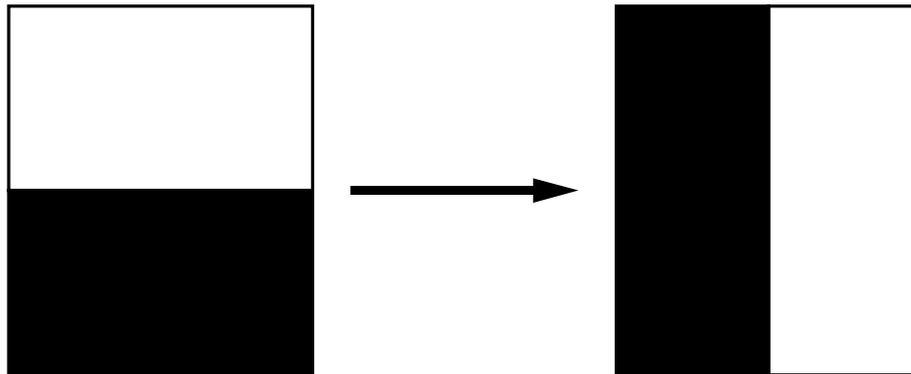
The following specifications apply for: VSS=0V, VDD=3.3V, TOPR =25°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------------|----------|--------------|----------------|---------|------|---------|------|
| Logic supply voltage | Vdd | - | VDD | 2.3 | 3.3 | 3.6 | V |
| High level input voltage | VIH | - | - | 0.7 Vdd | - | Vdd | V |
| Low level input voltage | VIL | - | - | 0 | - | 0.3 Vdd | V |
| High level output voltage | VOH | IOH = 400uA | - | Vdd-0.4 | - | - | V |
| Low level output voltage | VOL | IOL = -400uA | - | 0 | - | 0.4 | V |
| OTP Program voltage | VPP | - | VPP | - | 7.8 | - | V |
| Typical power panel | PTYP | - | - | - | 49.5 | - | mW |
| Deep sleep mode | PSTPY | - | - | - | 3.3 | - | uW |
| Typical operating current | Iopr_VDD | Vdd =3.3V | - | - | 15 | - | mA |

| | | | | | | | |
|---------------------------------|----------|---|-----|-----|----|------|-----|
| Sleep mode current | Islp_VDD | VDD=3.3V DC/DC OFF No clock No output load Ram data retain | VDD | - | 35 | -- | uA |
| Deep sleep mode current | IdslpVDD | VDD=3.3V DC/DC OFF No clock No output load Ram data not retain | VDD | - | 1 | -- | uA |
| Operation temperature range | TOPR | - | - | 0 | - | 50 | °C |
| Operation illuminance intensity | E | indoor only | - | - | - | 2000 | lux |
| Storage temperature range | TSTG | - | - | -25 | - | 60 | °C |
| Storage relative humidity | RHst | - | - | 30 | - | 60 | %RH |

Notes: 1. The typical power is measured with following transition:from horizontal 2 gray scale pattern tovertical 2 gray scale pattern. (Figure 10-2)

Figure 10-2 The typical power consumption measure pattern



- 2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- 3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform providedby SID.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.3V, TOPR =25°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------|--------|-----------|----------------|------|------|------|------|
| VCOM output voltage | VCOM | - | VCOM | -3.0 | - | -0.2 | V |

6.4 Panel AC Characteristics

MCU Interface Selection

JS0750NW20-MNG-A0 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

| BS | Interface | CSB | DC | SCL | SDA |
|------|------------|-----------|------------|-----------|-----------|
| High | 3-wire SPI | Available | Fix to GND | Available | Available |
| Low | 4-wire SPI | Available | Available | Available | Available |

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

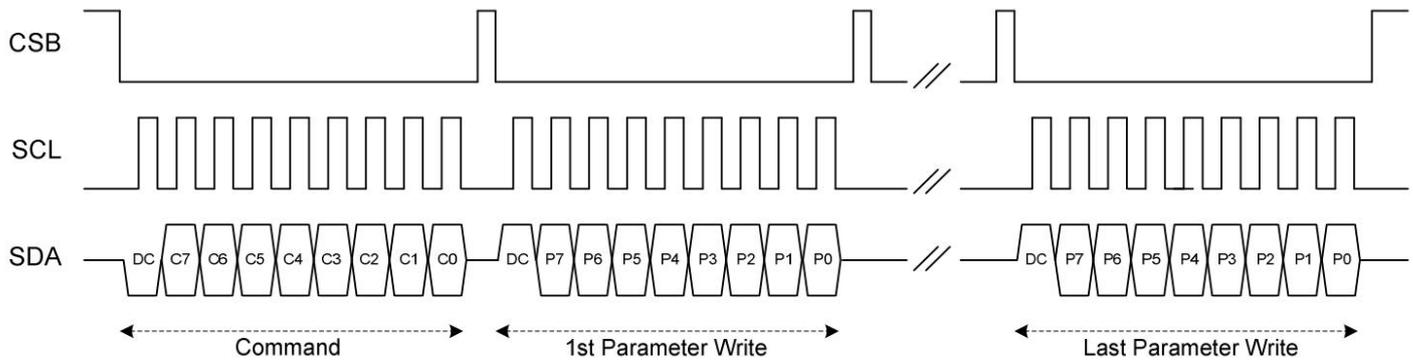


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

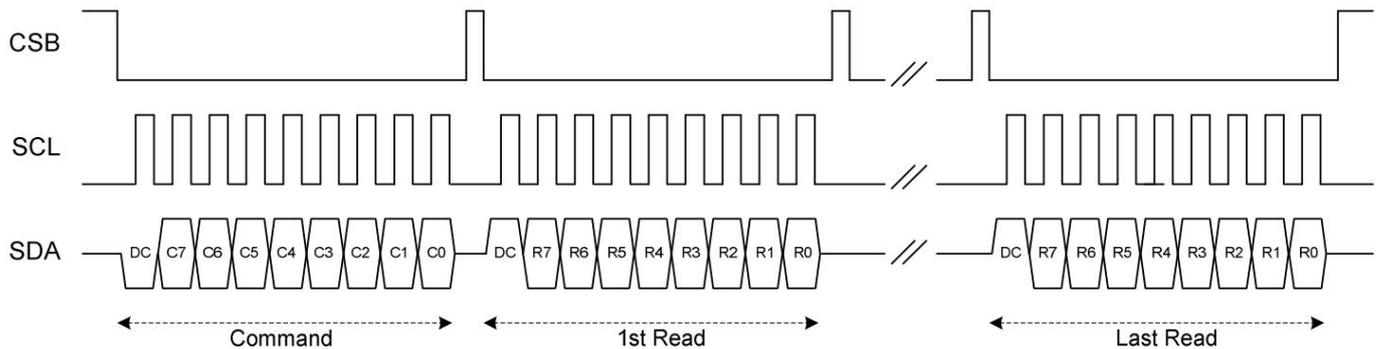


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

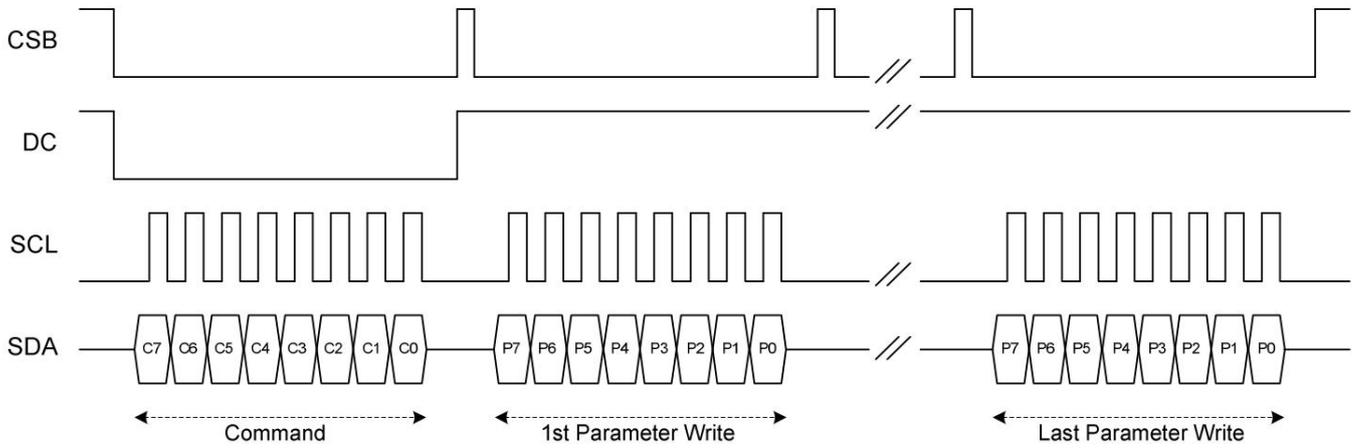


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

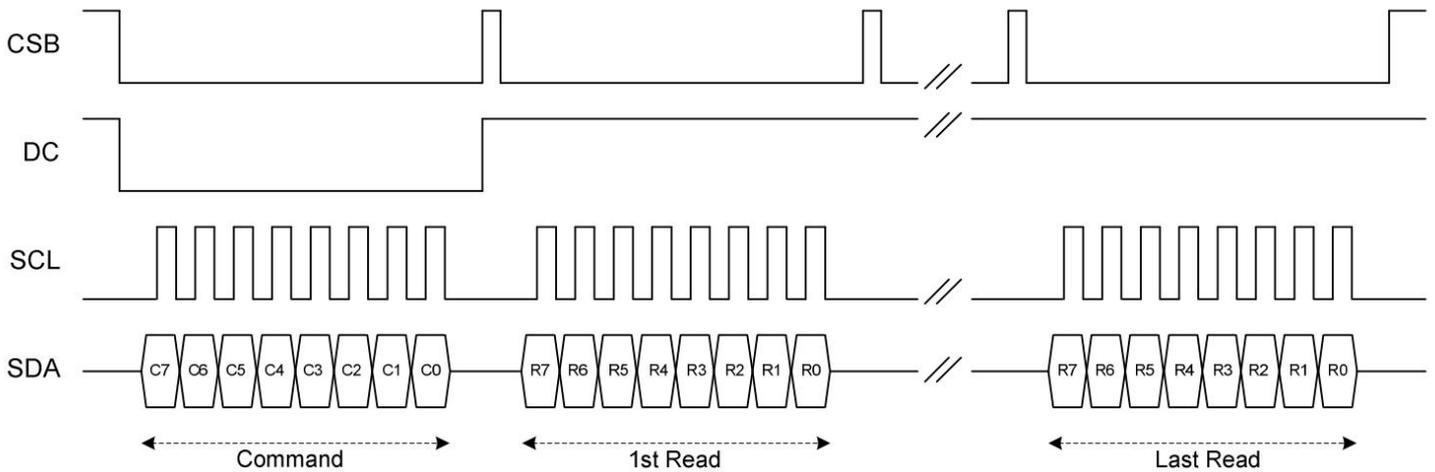


Figure: 4-wire SPI read operation

AC CHARACTERISTICS

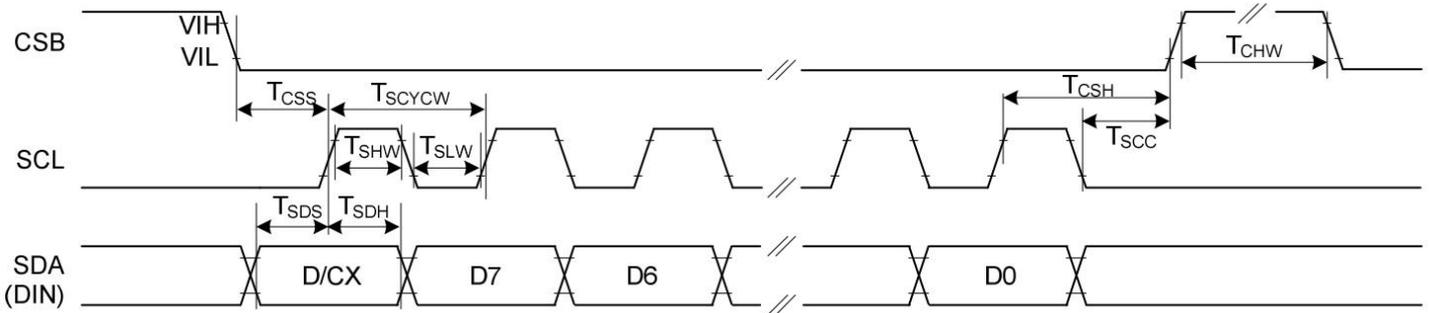


Figure: 3-wire Serial Interface Characteristics (Write mode)

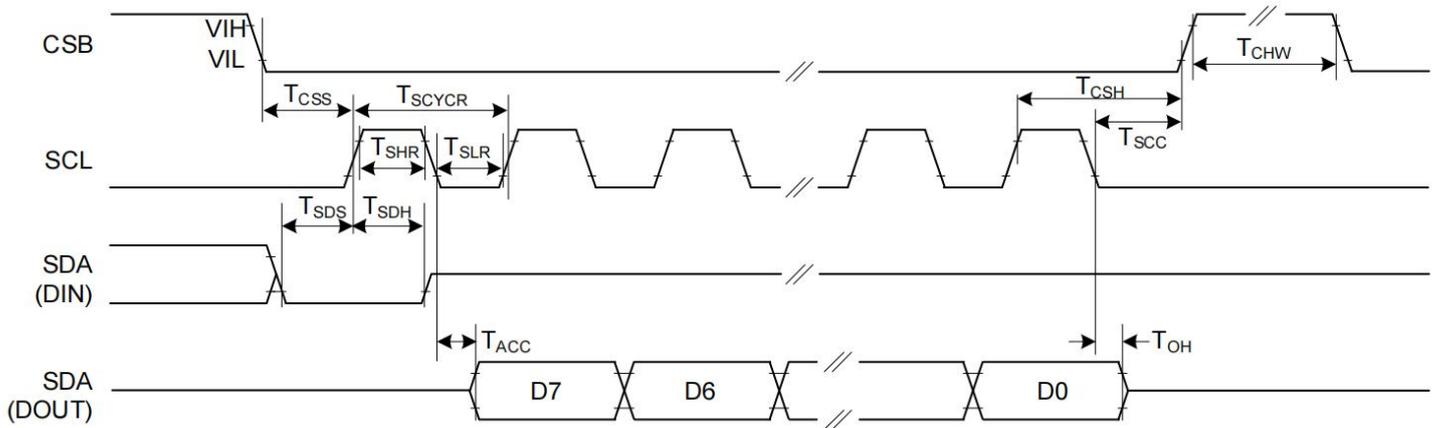


Figure: 3-wire Serial Interface Characteristics (Read mode)

| Symbol | Signal / Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------|-----------------------------|------|------|------|------|
| T_{CSS} | CSB | Chip select setup time | 60 | | | ns |
| T_{CSH} | | Chip select hold time | 65 | | | ns |
| T_{SCC} | | Chip select setup time | 20 | | | ns |
| T_{CHW} | | Chip select setup time | 40 | | | ns |
| T_{SCYCW} | SCL | Serial clock cycle (Write) | 100 | | | ns |
| T_{SHW} | | SCL "H" pulse width (Write) | 35 | | | ns |
| T_{SLW} | | SCL "L" pulse width (Write) | 35 | | | ns |
| T_{SCYCR} | | Serial clock cycle (Read) | 230 | | | ns |
| T_{SHR} | | SCL "H" pulse width (Read) | 110 | | | ns |
| T_{SLR} | | SCL "L" pulse width (Read) | 110 | | | ns |
| T_{SDS} | SDA (DIN) | Data setup time | 30 | | | ns |
| T_{SDH} | | Data hold time | 30 | | | ns |
| T_{ACC} | SDA (DOUT) | Access time | | | 230 | ns |
| T_{OH} | | Output disable time | 15 | | | ns |

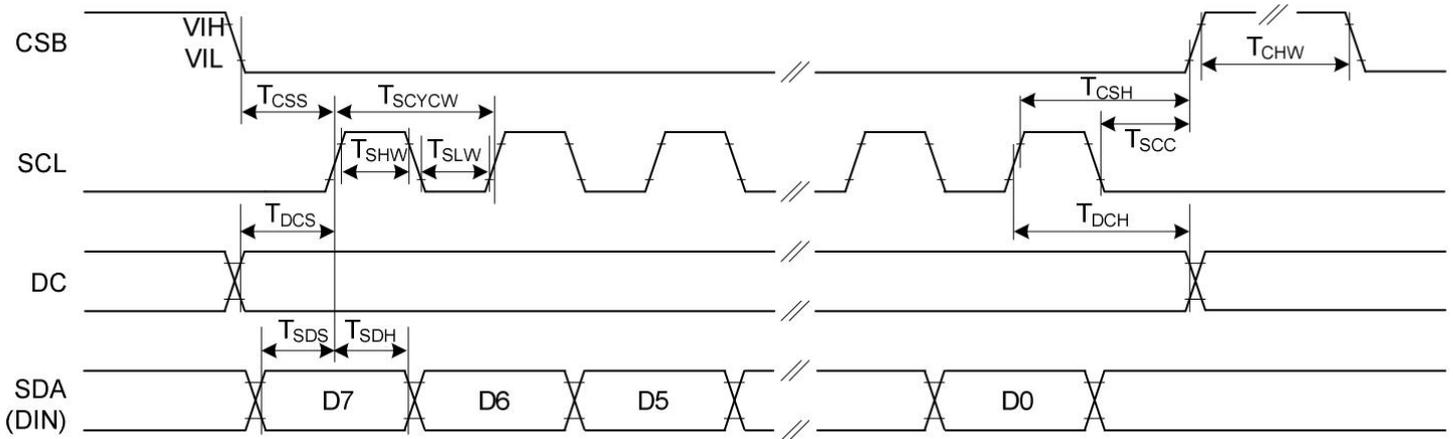


Figure: 4-wire Serial Interface Characteristics (Write mode)

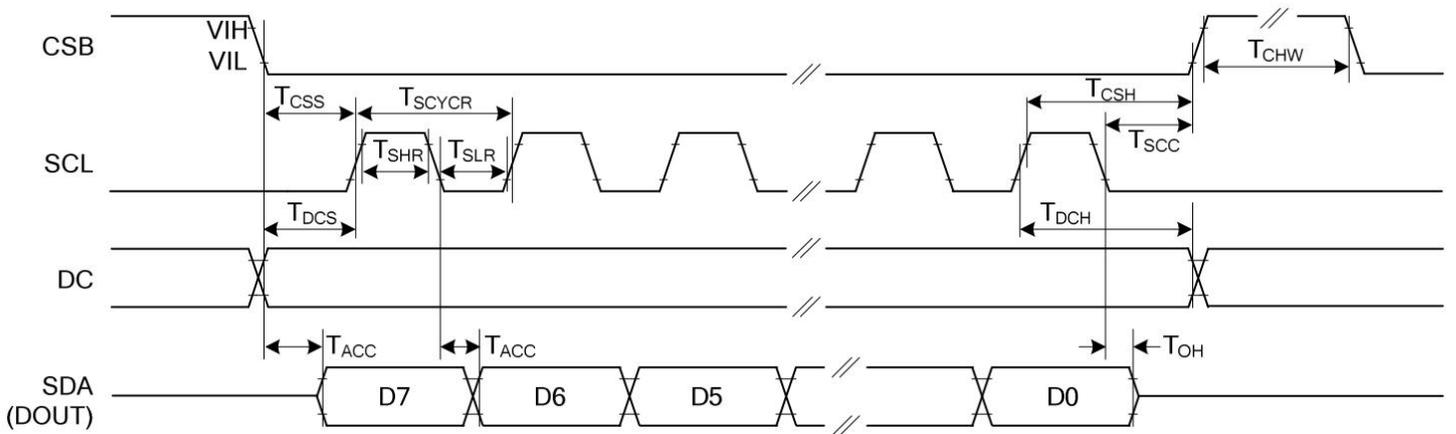


Figure: 4-wire Serial Interface Characteristics (Read mode)

| Symbol | Signal / Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|--------------------|-----------------------------|------|------|------|------|
| T _{CSS} | CSB | Chip select setup time | 60 | | | ns |
| T _{CSH} | | Chip select hold time | 65 | | | ns |
| T _{SCC} | | Chip select setup time | 20 | | | ns |
| T _{CHW} | | Chip select setup time | 40 | | | ns |
| T _{SCYCW} | SCL | Serial clock cycle (Write) | 100 | | | ns |
| T _{SHW} | | SCL "H" pulse width (Write) | 35 | | | ns |
| T _{SLW} | | SCL "L" pulse width (Write) | 35 | | | ns |
| T _{SCYCR} | | Serial clock cycle (Read) | 230 | | | ns |
| T _{SHR} | | SCL "H" pulse width (Read) | 110 | | | ns |
| T _{SLR} | | SCL "L" pulse width (Read) | 110 | | | ns |
| T _{DCS} | DC | DC setup time | 30 | | | ns |
| T _{DCH} | | DC hold time | 30 | | | ns |
| T _{SDS} | SDA (DIN) | Data setup time | 30 | | | ns |
| T _{SDH} | | Data hold time | 30 | | | ns |
| T _{ACC} | SDA (DOUT) | Access time | | | 230 | ns |
| T _{OH} | SDA (DOUT) | Output disable time | 15 | | | ns |

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

| Symbol | Parameter | Conditions | Values | | | Units | Notes |
|-------------|--------------------|------------|--------|------|-----|-------|-------|
| | | | Min. | Typ. | Max | | |
| R | White Reflectivity | White | 30 | 35 | - | % | 7-1 |
| CR | Contrast Ratio | | 8:1 | 10:1 | - | - | 7-2 |
| White L 24h | Reduce | | - | ≤4 | - | - | - |
| Tupdate | Image update time | at 25 °C | - | TBD | - | ms | - |

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

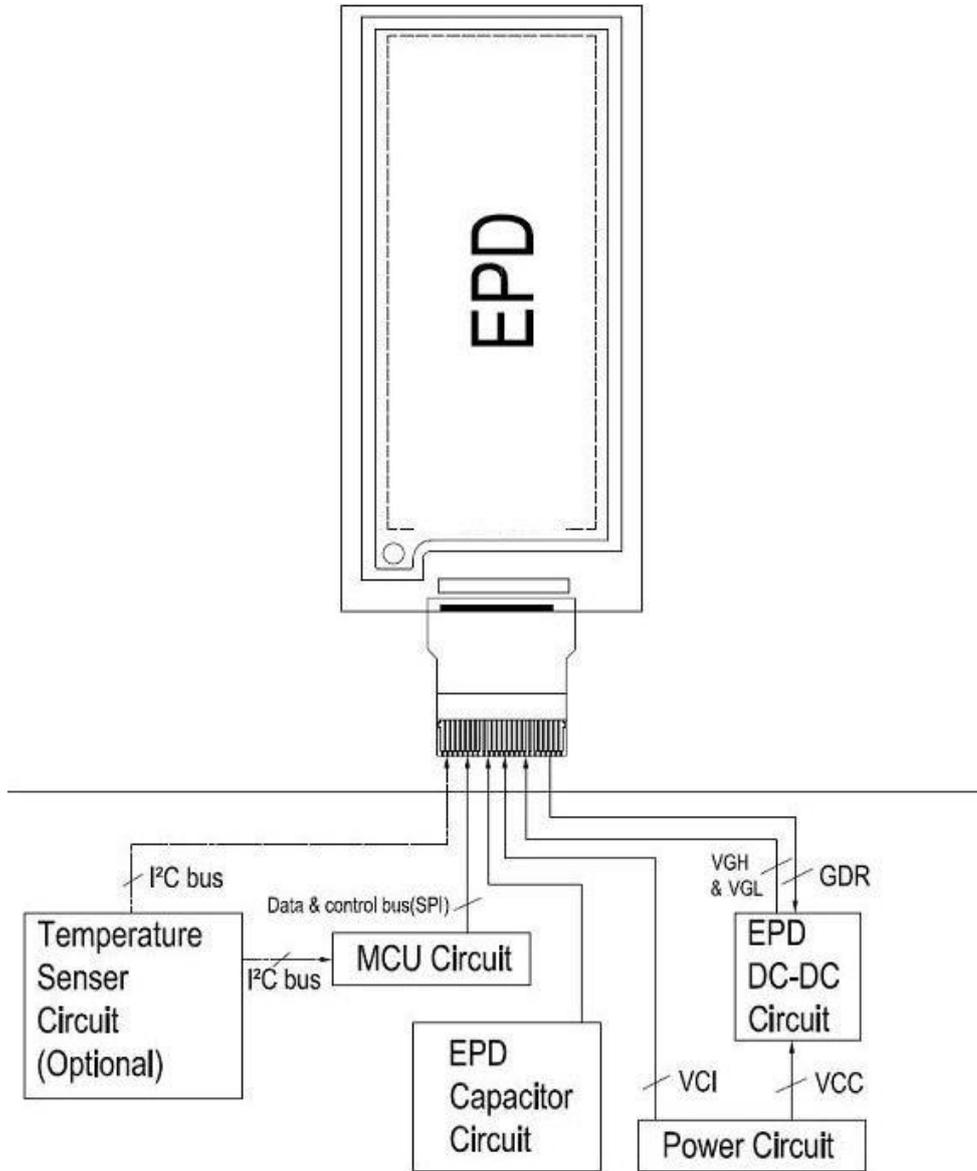
8 Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15°C to 35°C, and humidity from 30%RH to 60%RH.
- 12.

9 Reliability Test

| No. | Test | Condition | Method | Remark |
|-----|---|---|-------------------------|--|
| 1 | High-Temperature Operation | T = +50°C, RH = 30% for 168 hrs | IEC 60 068- 2- 2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 2 | Low-Temperature Operation | T = 0°C for 168 hrs | IEC 60 068- 2- 2Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 3 | High-Temperature Storage | T = +70°C, RH=23% for 168 hrs | IEC 60 068- 2- 2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 4 | Low-Temperature Storage | T = -25°C for 168 hrs | IEC 60 068- 2- 1Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 5 | High-Temperature, High-Humidity Operation | T = +40°C, RH = 90% for 168 hrs | IEC 60 068- 2- 3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 6 | High Temperature, High-Humidity Storage | T = +60°C, RH=80% for 168hrs | IEC 60 068- 2- 3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 7 | Thermal Shock | 1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles | IEC 60 068-2-14 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 8 | Package Vibration | 1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction | Full packedfor shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 9 | Package Drop Impact | Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each | Full packedfor shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 10 | Electrostatic Effect (non-operating) | Machine model +/- 250V, 0Ω, 200pF | IEC 62179, IEC 62180 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |

10 Block Diagram

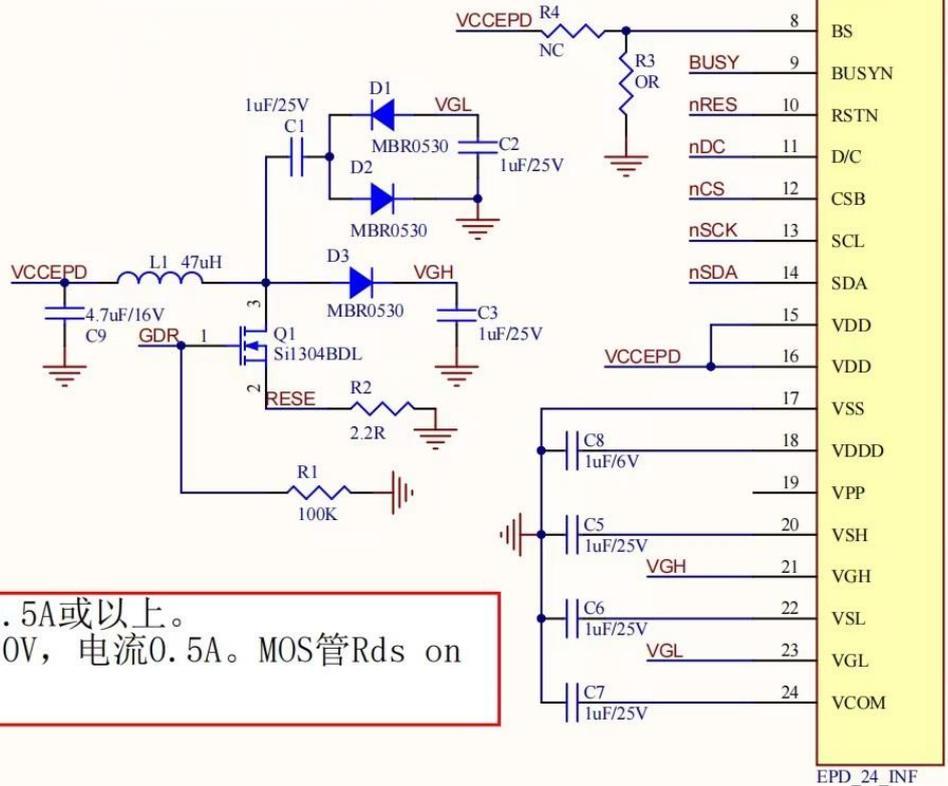


Driver PCBA

11 Typical Application Circuit with SPI Interface

1. Power Inductor: 47uH, I > 500mA
2. Switch MOS NMOS : V_{ds} ≥ 30V, I_d > 500mA, R_{ds(on)} < 2.1Ω, V_{gs} = 2.5V
3. Schottky Diode: V_r ≥ 30V, I_f > 500mA

EPD DEMO CIRCUIT



(1) 功率电感用47uH，电流0.5A或以上。
 (2) MOS管和二极管具：耐压30V，电流0.5A。MOS管R_{ds on} ≤ 2.1Ω @ V_{gs} = 2.5V。

数字化无纸化办公系统的规格参数



- 基本参数：**
 产品名称：数字化智能化7.5吋三色/四色电子门牌
 产品型号：|
 产品尺寸：185.4×126.4×13mm
 显示技术：电子纸显示技术
 可视区域：162.4×97.12mm
 分辨率：800×480
 显示颜色：黑/白/红三色；黑/白/红/黄四色
 视角：接近180°，可双面不同画面显示
 工作电压：3.7V
 通讯方式：蓝牙通讯
 频率范围：2.4GHz（蓝牙5.0）
 传输距离：网关/手机10米区域（无遮挡）
 接收灵敏度：-80dBm（受实际环境影响，以实测为准）
 功耗：数据传输平均电流6mA，待机160uA
 产品净重：299±5g
 产品材质：ABS+PC，
 外观颜色：白色
 供电方式：内置电池
 电池型号：充电锂电池，5000mAh；
 续航：8个月/充电一次（按每天刷新5次计算）
 使用温度：0℃-50℃