

SHEN ZHEN JICTECH LCD CO., LTD.

产品规格书 Product Specification

产品名
Product
TFT-LCD OPEN CELL

机种名 Model JH215IALKN-01

【接收印栏】			

- ※ 本基准书由封面、附件等全_22_页构成。 如果对该规格书有异议,请在下订单前提出。
- * This Product Specification have <u>22</u> pages including the coversheet and Appendices. Please negotiate the objection point before purchase order.

研发中心 设计整合部

R&D CENTER, DESIGN INTEGRATION SECTION.

- CONTENTS -

REVISION HISTORY	3
1. GENERAL DESCRIPTION 1.1 OVERVIEW 1.2 CHARACTERISTICS 1.3 PIXEL ARRAY MEMBER LOCATION	4
2. ABSOLUTE MAXIMUM RATINGS 2.1 ABSOLUTE RATINGS OF ENVIRONMENT	5
3. ELECTRICAL CHARACTERISTICS 3.1 ABSOLUTE MAXIMUN RATING 3.2 CONTROL CIRCUIT DRIVING	6
4. INTERFACE PIN CONNECTION 4.1 TFT LCD OPEN CELL 4.2 BLOCK DIAGRAM (OPEN CELL) 4.3 LVDS INTERFACE 4.4 COLOR DATA INPUT ASSIGNMENT	8
5. INTERFACE TIMING 5.1 INPUT SIGNAL TIMING SPECIFICATIONS	12
6. OPTICAL CHARACTERISTICS 6.1 OPTICAL SPECIFICATION	14
7. DEFINITIONS OF LABELS 7.1 MULTI-CELL LABAL 7.2 OPEN-CELL LABEL 7.3 CELLBOX LABEL	17
8. Packing 8.1 PACKING SPECIFICATIONS 8.2 PACKING METHOD	18
9. PRECAUTIONS	18
10. RELIABILITY TEST ITEMS	20
11. MECHANICAL DRAWING	20

REVISION HISTORY

DATE	REVISED No.	PAGE	SUMMARY	NOTE
2015/02/02	AV1.0	20	First Edition	Final
2015/05/13	AV1.1	20	P14: Add Transmittance spec	Final
2015/09/10	AV1.2	4,6,12,14,15 ,16,17	P4: Adding the definition of O/S driving. P6:Adding the ICC and Power consumption with O/S driving. P12:Update the spread spectrum modulation range. P14:Adding the Response time with O/S driving. P15:Adding the note 4. P16: Adding the note 6. P17:Update the Cell Box Label.	
2015/12/04	AV1.3	4,18,22	P4:Add 0.7mm glass weight and multicell glass size. P18:Add 0.7mm glass's total mass of one EPS BOX filled with full panel. P22:Add 0.7mm glass mechanical drawing.	
			!	

1. GENERAL DESCRIPTION

1.1 OVERVIEW

This module is color active matrix LCD Open-cell incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, PWB. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with about 16.7M colors (R/G/B 6bits+Hi FRC data in each color) by using LVDS(Low Voltage Differential Signaling) to interface, +5V of DC supply voltage.

In order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

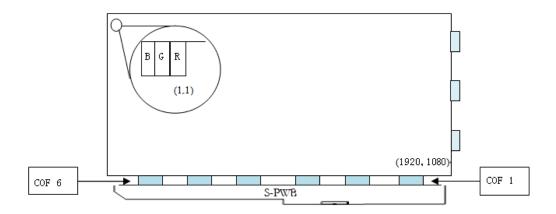
1.2 CHARACTERISTICS

CHARACTERISTICS ITEMS	SPECIFICATIONS					
Screen Diagonal [in]	21.5"					
Pixels [lines]	1920×1080					
Active Area [mm]	476.64 (H) x 268.11 (V)					
Pixel Pitch [mm]	0.24825 (H) x 0.24825 (V)					
Pixel Arrangement	RGB vertical stripe					
Waight [a]	420(0.5mm glass)					
Weight [g]	570(0.7mm glass)					
Physical Size(COF/PWB included) [mm]	487.54(H) x 318.86(V) x 2.9(D) Typ.					
Multi cell glace Size [mm]	487.54(H)x282.91(V) x1.34(D)Typ(0.5mm glass)					
Multi-cell glass Size [mm]	487.54(H)x282.91(V) x1.74(D)Typ(0.7mm glass)					
Display Mode(VA mode)	Normally Black					
Surface treatment (Without the protection film)	Anti-glare,3H					

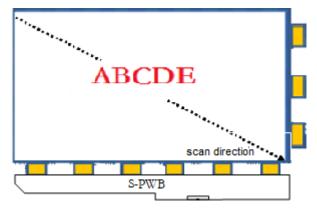
1.3 PIXEL ARRAY AND MEMBER LOCATION

Pixel array and member located as below.

There are 6 Source Drivers (960 input terminals S-Dr) on this panel.



Please use this Open Cell like following figure.



2. ABSOLUTE MAXIMUM RATINGS

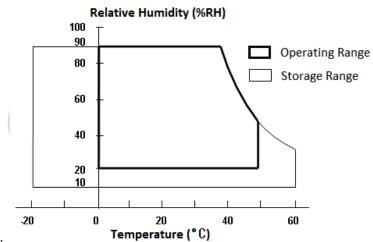
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Va	lue	Unit	Note	
item	Symbol	Min.	Max.	Offic	Note	
Storage Temperature	T _{ST}	-20	+60	°C	[Note1, 3]	
Operating Ambient Temperature	T _{OP}	0	50	°C	[Note1, 2, 3]	
Altitude Operating	A _{OP}	0	5000	М	[Note3]	
Altitude Storage	A _{ST}	0	12000	М	[Note3]	

Storage Condition: With shipping package.

[Note 1] Temperature and relative humidity range is shown in the figure below.

- *1) 90 %RH Max. (Ta \leq 40 °C).
- *2) Wet-bulb temperature should be 40 °C Max. (Ta > 40 °C).



- *3) No condensation.
- [Note 2] The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 50°C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 60°C. The range of operating temperature may degrade in case of improper thermal management in your product design.
- [Note 3] The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

3. ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Ratings	Unit	Remark
+5V supply voltage	VCC	Ta=25 ℃	0~+6	V	
Storage temperature	Tstg	-	-20~ + 60	${\mathbb C}$	
Operation temperature	Тора	-	0~+50	$^{\circ}$	

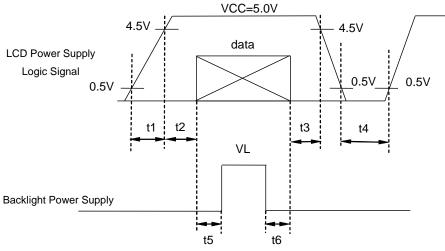
3.2 Control circuit driving

Parame	eter	Symbol	Min	Тур	Max	Unit	Remark
	Supply voltage	VCC	4.5	5.0	5.5	V	[Note 1]
			-	900	1000	mA	VCC=5.0V,60Hz White Pattern
+5V supply voltage	Current dissipation	ICC	-	1000	1150	mA	VCC=5.0V,60Hz White Pattern O/S Driving
		Irush	-	-	3	А	[Note 2]
Permissible input	ripple voltage	VRP	-	-	300	mVp-p	VCC=5.0V
Differential Input	High	VTH	-	-	100	mV	VCM=1.2V
Threshold Voltage	Low	VTL	-100	-	-	mV	[Note 3]
Input Different	ial Voltage	VID	100	-	600	mV	[Note 3]
Differential Inpu Mode Vo		VCM	1.0	1.2	1.5	V	[Note 3]
Dower	umntion	Р	-	4.5	5.0	W	Without O/S Driving
Power cons	umption	P	-	5.0	5.75	W	With O/S Driving

[VCM]: Common mode voltage of LVDS driver

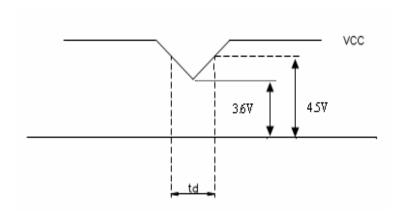
[Note1] Power, data sequence

 $0.50 ms \le t1 \le 10 ms$ $t4 \ge 1 sec$ $0.01 ms < t2 \le 50 ms$ $t5 \ge 500 ms$ $0.01 ms < t3 \le 50 ms$ $t6 \ge 200 ms$



Data: RGB DATA, DCLK, DENA

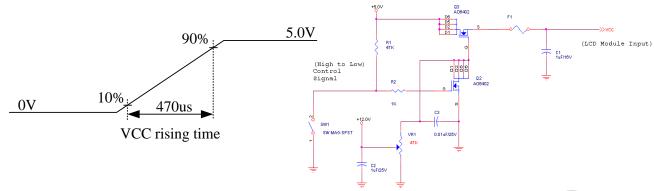
- Data: CLKIN±,RIN0±,RIN1±, RIN2±, RIN3±
- About the relation between data input and back light lighting, please base on the above-mentioned input sequence.
- When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.
- ★ VCC-dip conditions:
 - (1) When $3.6V \le VCC(min) < 4.5V$, $td \le 10 ms$
 - (2) When VCC <3.6 V, VCC-dip conditions should also follow the VCC-turn-on conditions.



[Note2]

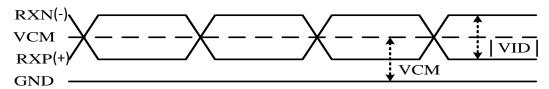
Irush Measurement Condition:

The duration of rising time of power input is 470us.

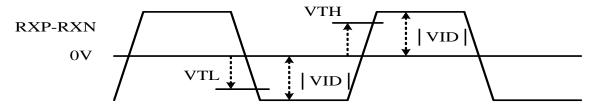


[Note 3] CLKIN+/CLKIN-, RIN0+/RIN0-, RIN1+/RIN1-, RIN2+/RIN2-, RIN3+/RIN3-

[Single-end Signals]



[Differential Signal]



4. INTERFACE PIN CONNECTION

4.1 TFT LCD OPEN CELL

CN1 (Interface signals and +5V DC power supply) Shown on the next table.

Using connector: MSCKT2407P30HB (STM) or compatible

Matching connector: PK2407P30W (STM) or compatible

Pin No.	Symbol	Function	Remark
1	RxOIN0-	Negative LVDS DATA input(ODD)	LVDS
2	RxOIN0+	Positive LVDS DATA input(ODD)	LVDS
3	RxOIN1-	Negative LVDS DATA input(ODD)	LVDS
4	RxOIN1+	Positive LVDS DATA input(ODD)	LVDS
5	RxOIN2-	Negative LVDS DATA input(ODD)	LVDS
6	RxOIN2+	Positive LVDS DATA input(ODD)	LVDS

7	GND	Ground	
8	RxOCLK-	Negative LVDS Clock input(ODD)	LVDS
9	RxOCLK+	Positive LVDS Clock input(ODD)	LVDS
10	RxOIN3-	Negative LVDS DATA input(ODD)	LVDS
11	RxOIN3+	Positive LVDS DATA input(ODD)	LVDS
12	RxEIN0-	Negative LVDS DATA input(EVEN)	LVDS
13	RxEIN0+	Positive LVDS DATA input(EVEN)	LVDS
14	GND	Ground	
15	RxEIN1-	Negative LVDS DATA input(EVEN)	LVDS
16	RxEIN1+	Positive LVDS DATA input(EVEN)	LVDS
17	GND	Ground	
18	RxEIN2-	Negative LVDS DATA input(EVEN)	LVDS
19	RxEIN2+	Positive LVDS DATA input(EVEN)	LVDS
20	RxCLK-	Negative LVDS Clock input(EVEN)	LVDS
21	RxCLK+	Positive LVDS Clock input(EVEN)	LVDS
22	RxEIN3-	Negative LVDS DATA input(EVEN)	LVDS
23	RxEIN3+	Positive LVDS DATA input(EVEN)	LVDS
24	GND	Ground	
25	NC	No connection(Do not connect)	
26	NC	No connection(Do not connect)	
27	NC	No connection(Do not connect)	[Note 1]
28	VDD	POWER +5V	
29	VDD	POWER +5V	
30	VDD	POWER +5V	

[Note 1] Built-in Self Test (BIST)

*1) PIN27=NC: Disable BIST function.

Available LVDS Signal input: Display LVDS input Pattern.

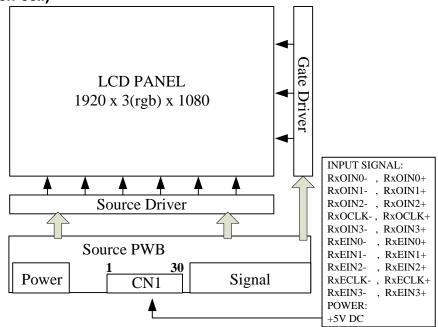
No LVDS Signal or unavailable LVDS Signal input: Display Black Pattern.

*2) PIN27=High(2.7V~3.3V): Enable BIST function.

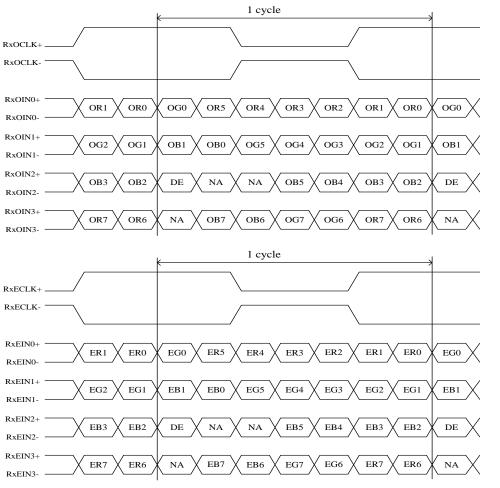
Available LVDS Signal input: Display LVDS input Pattern.

No LVDS Signal or unavailable LVDS Signal input: Display BIST Pattern.

4.2 Block Diagram (Open-cell)



4.3 LVDS INTERFACE



DE: Display Enable

NA: Not Available (Fixed Low)

4.4 COLOR DATA INPUT ASSIGNMENT

		-		Data signal																						
	Colors & Gray scale	Gray Scale	R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	В3	B4	B5	В6	В7
	Black	_	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	_	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
o r	Green	_	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic Color	Cyan	_	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
asic	Red	_	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
В	Magenta	_	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	_	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	_	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
_	Û	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rec	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
le of	Û	←				7	r							,	L							,	V			
Sca	û û ↑				1	L								L							,	V				
Gray Scale of Red	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ĭ	û	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
n n	Û	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
e of	Û	V				1	V								L							,	V			
Scal	û	\downarrow				-	V								V							•	V			
ray	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
G	û	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
o	Û	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Blu	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray Scale of Blue	Û	→				1	V				V								,	V						
Scal	û	→					V								V								V			
ray	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
G	û	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

0: Low level voltage,

1: High level voltage.

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,7M colors display can be achieved on the screen.

5. INTERFACE TIMING

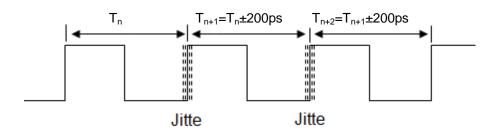
5.1 INPUT SIGNAL TIMING SPECIFICATIONS

(a) The input signal timing specifications are shown as the following table and timing diagram.

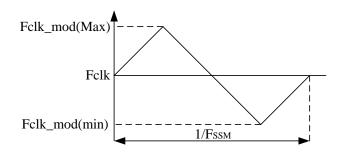
		Ite	em	Symbol	Min	Тур.	Max.	Unit
			Freq.	fCLK	55	72	90	MHz
	DCLK		Cycle	tCLK	18.18	13.89	11.11	ns
			Input cycle to cycle jitter	T _{RCL}	-	-	200	ps
		DCLK	Spread Spectrum Modulation range	F _{clk_mod}	Fclk-2%	-	Fclk+2%	MHz
LCD		Spread Spectrum Modulation frequency	Fssm	30	-	100	KHz	
Timing			Horizontal effective time	tHA	960	960	960	tCLK
		Horizontal	Horizontal blank time	tHB	32	100	115	tCLK
			Horizontal total time	tH	992	1060	1075	tCLK
	DE		Vertical frame Rate	Fr	50	60	75	Hz
		Vertical	Vertical total time	tV	1084	1130	1170	tH
		vertical	Vertical effective time	tVA	1080	1080	1080	tH
			Vertical blank time	tVB	4	50	90	tH

[Note]

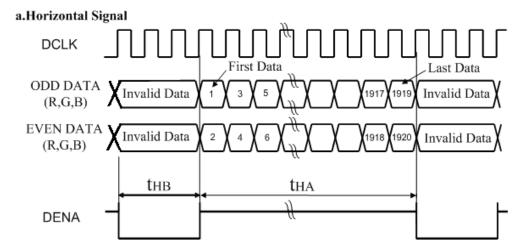
- *1) DE (data enable) usually is positive.
- *2) DCLK still inputs during blanking.
- *3) DE mode only.
- *4) It may cause flicker at 50Hz.
- *5) The input cycle to cycle jitter is defined as below figure, $T_{RCL} = |T_{n+1} T_n|$

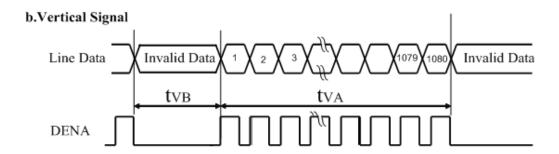


*6) SSCG (Spread spectrum clock generator) is defined as following.



(b) Timing Chart





6. OPTICAL CHARACTERISTICS

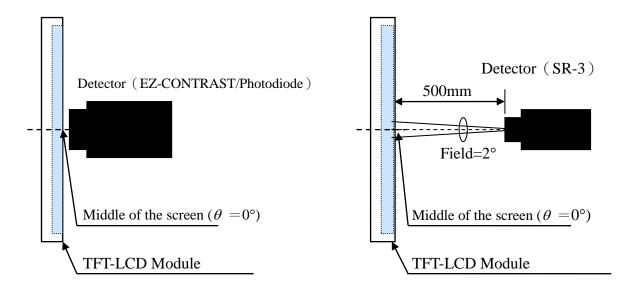
6.1 OPTICAL SPECIFICATION

Ta=25°C

Parar	neter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark	
		θ 21		-	88	-	Deg.		
Viewing	Horizontal	θ 22		-	88	-	Deg.		
angle range		θ 11	CR>10	-	88	-	Deg.	[Note1,4]	
	Vertical	θ 12		-	88	-	Deg.		
Contra	st ratio	CR		-	3000	-	-	[Note2,4]	
Dannana tima		Tr+Tf		-	25	-	ms	[Note3,5]	
Respon	Response time			-	8	-	ms	[Note4,5,6]	
Chromatici	ty of white	Х			0.313		-		
Chromatici	ty or write	у			0.329		-		
Chromatic	city of red	Х	θ =0 deg.		0.646		-		
Cilionian	only of red	у		Typ0.03	0.347	Typ.+0.03	-		
Chromatici	ty of green	Х		тур0.03	0.322	тур.+0.03	-	[Note 4]	
Cilionalici	ty or green	у			0.630		-		
Chromatic	Chromaticity of blue				0.155		-		
Ciliomatic					0.061		-		
Transm	ittance	Т		3.4	4.0	-	%		

^{*}The measurement shall be executed 30 minutes after lighting at rating.

^{*} The optical characteristics are measured using the following equipment.

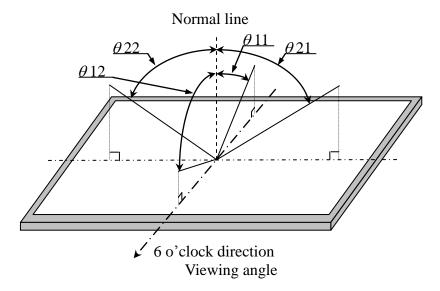


Measurement of viewing angle range, Response time.

Measurement of Contrast, Luminance, Chromaticity.

^{*}These values are measured with CPL standard back light unit.

[Note 1] Definitions of viewing angle range:

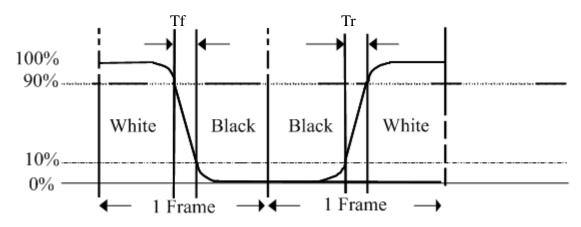


[Note 2] Definition of contrast ratio:

The contrast ratio is defined as the following.

[Note 3] Definition of response time

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time, Tr), and from "Full White" to "Full Black" (falling time, Tf), respectively. The response time is interval between the 10% and 90% (1 frame at 60 Hz) of amplitudes.



Response time=Tr+ Tf

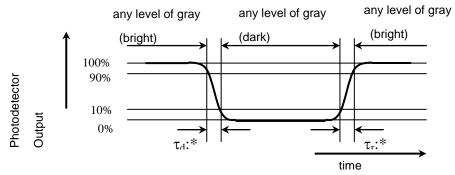
[Note 4] Definition of response time

The response time (τ_{DRV}) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%) and "any level of gray (0%, 25%, 50%, 75% and 100%).

	0%	25%	50%	75%	100%
0%		τ_r :0%–25%	τ _r :0%–50%	τ _r :0%–75%	τ _r :0%–100%
25%	τ _d :25%–0%		τ _r :25%–50%	τ _r :25%–75%	τ _r :25%–100%
50%	τ _d :50%–0%	τ_d :50%–25%		τ _r :50%–75%	τ _r :50%–100%
75%	τ _d :75%–0%	τ_d :75%–25%	τ _d :75%–50%		τ _r :75%–100%
100%	τ _d :100%–0%	τ _d :100%–25%	τ _d :100%–50%	τ _d :100%–75%	

 $\tau^*\text{:}x\text{-}y\text{...}\text{response}$ time from level of gray(x) to level of gray(y)

$$\tau_{DRV} = \Sigma (\tau^*:x-y)/20$$



[Note 5] This shall be measured at center of the screen.

[Note 6] This value is valid when O/S driving is used at typical input time value.

7. DEFINITIONS OF LABELS

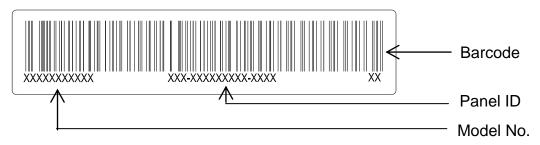
7.1 MULTI-CELL LABEL

The label of Multi-cell sticks on the front side of the panel.

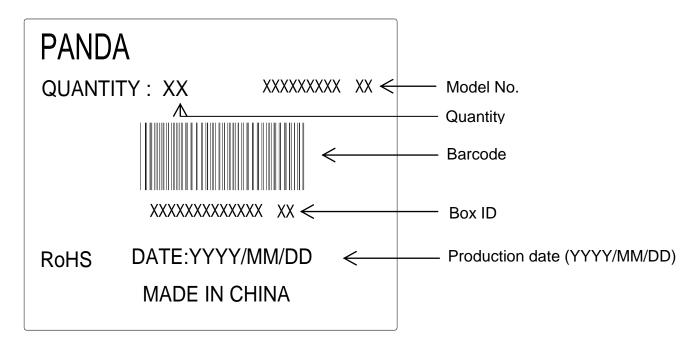


7.2 OPEN CELL LABEL

The label of Open-cell sticks on the non-component side of the PWB.



7.3 CELL BOX LABEL



8. PACKING

8.1 PACKING SPECIFICATIONS

(a) Piling number of EPS BOX : 2x2 columns, 6 rows

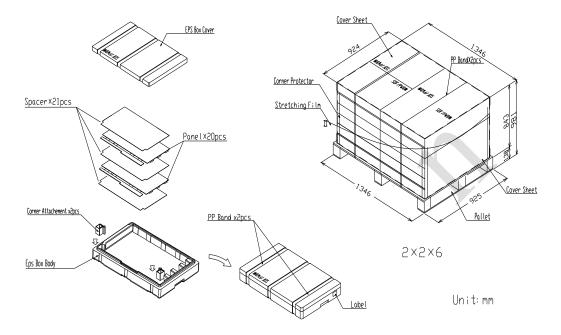
(b) Packing quantity in one ESP BOX : 20 pieces

 (c) EPS BOX size
 : 660mm*445mm*143mm

 (d) Pallet size
 : 1346mm*925mm*138mm

(e) Total mass of one EPS BOX filled with full Panel : 10.2kg(0.5mm glass) or 12.6kg(0.7mm glass)*

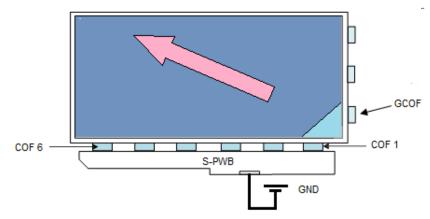
8.2 PACKING METHOD



9. PRECAUTIONS

- (a) Because the Open-Cell is too weak to destroy by static electricity, please don't touch the terminal with bare hands.
- (b) Front polarizer can easily be damaged. Pay attention on it.
- (c) Since long contact with drops of water may cause discoloration or spots, please wipe off them as soon as possible.
- (d) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- (e) The Panel will be broken or chipped when it is dropped or bumped against a hard substance.
- (f) Precautions of peeling off the Protection Film:
 - *1) Be sure to peel off slowly (recommended more than 7 sec.) and constant speed.
 - *2) Peeling direction shown in the next Fig.
 - *3) Be sure to ground person with adequate methods such as the anti-static wrist band.
 - *4) Be sure to connect PWB to GND while peeling off the protection film.
 - *5) Ionized air should be blown to the surface while peeling off the protection film.
 - *6) The protection film must not touch drivers and PWB.

 After the protection film has been peeled off, some adhesive may be remained on the polarizer. Please use isopropyl-alcohol to remove it.
 - *7) The protection film should not be peeled off casually and pasted back.



- (g) Since the Open-cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling an Open-Cell should be grounded though adequate methods such as an anti-static wrist band. Connector pins should not be touched directly with bare hands.
- (h) Avoiding COF damage, do not bend PWB to display side when handling the open cell, recommend coating silicon or tuffy on front and back side of COF.

Reference: Process control standard of CPL.

	item	Management standard value and performance standard
1	Anti-static mat(shelf)	1to50 [Mega ohm]
2	Anti-static mat(floor, desk)	1to100 [Mega ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within two seconds.
4	Anti-static wrist band	0.8 to 10 [Mega ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [°C]
7	Humidity	60 to 70 [%]

- (i) Since the Open-cell has a PWB, please take care to keep it off any stress or pressure when handling or installing the Open-cell, otherwise some of electronic parts on them may be damaged.
- (j) Be sure to turn off the power supply when inserting or disconnecting the cable.
- (k) Be sure to design the module and cabinet so that the Open-cell van is installed without any extra stress such as warp or twist.
- (1) When handling and assembling Open-Cell into module, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of materials such as reagent, solvent, adhesive, resin... etc, which generate these gasses, may cause corrosion and discoloration of the Open-Cell.
- (m) Applying too much force and stress to PWB and drivers may cause a malfunction electrically and mechanically.
- (n) The Open-cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufactures.
- (o) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
- (p) The chemical compound, which causes the destruction of ozone layer, is not being used.
- (q) This Open-Cell module is corresponded to RoHS.
- (r) When any question or issue occurs, it shall be solved by mutual discussion.

10. RELIATBILITY TEST ITEMS

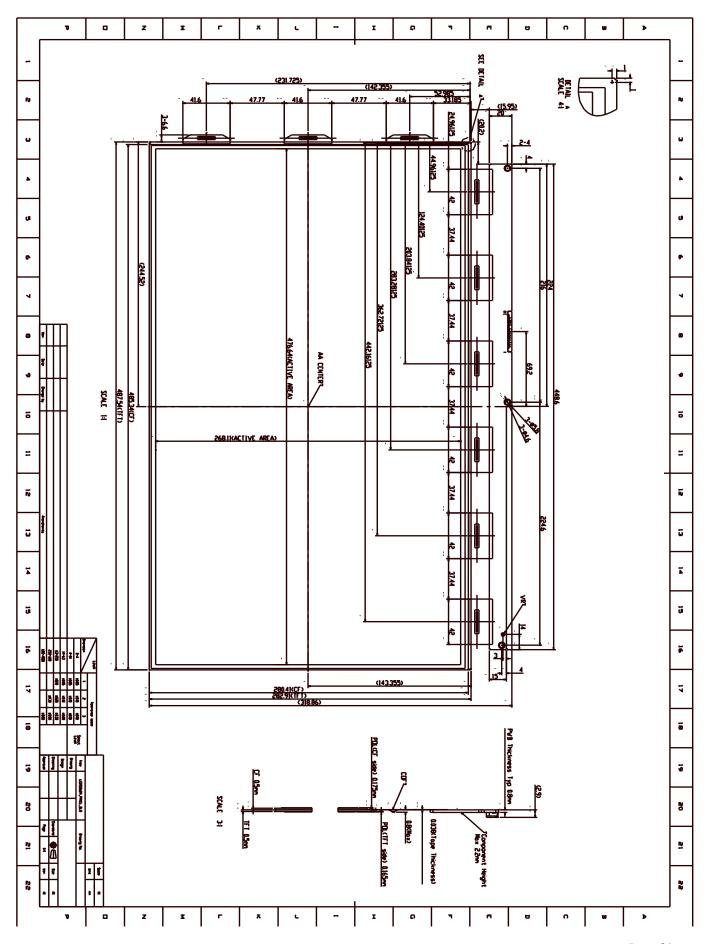
Test item	Condition	
High temperature storage test	Ta= 60°C, 240h	
Low temperature storage test	Ta=-20°C, 240h	
High temperature and high humidity operation test	Ta= 50°C, 80%RH, 240h (No condensation)	
High temperature operation test	Ta= 50°C, 240h	
Low temperature operation test	Ta= 0°C, 240h	
ESD(no operation)	Contact discharge on LVDS connector ±200V (200PF,0Ω)	

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

11. MECHANICAL DRAWING

a) 0.5mm glass



Page 21

a) 0.7mm glass

